CMOS 8-BIT MICROCONTROLLER

TMP90CR74ADF

1. OUTLINE AND CHARACTERISTICS

The TMP90CR74A is a high-performance 8-bit single-chip microcontroller; TLCS-90 CPU core capacious ROM, RAM and peripheral circuits adequate to control VCR system are included.

(1) Efficiently systematized instructions
- 163 instructions
- Multiplication, division, 16-bit arithmetic operation, Bit manipulation

(2) Minimum instruction execution time : 250 ns (at 16MHz Oscillation), 122 μs (at 32.8 kHz Oscillation.)

(3) Internal ROM : 56K bytes

(4) Internal RAM : 1K bytes

(5) 20-bit time-base Counter (TBC)

(6) 8-bit timer / counter : 4 channels
- Timer mode / Event counter mode
- 16-bit timer/counter mode

(7) Capture inputs : 8 terminals
- 18-bit timing data + 6-bit trigger data (with 8 level FIFO) : 1 channel
- 16-bit timing data + 1-bit trigger data : 2 channels

(8) Timing Pulse Generator (TPG) : 2 channels : 1 channel
- 16-bit timing data + 6-bit output data (with 4 level FIFO) : 1 channel
- 16-bit timing data + 4-bit output data

(9) PWM output
- 12-bit PWM : 2 channels
- 8-bit or 14-bit PWM : 1 channel

(10) C-Sync signal separation
- H/V SYNC separation
- Mute Detection

(11) VISS/VASS detection
- Index Search/Address code Search

(12) Head amp/Color rotary control circuit

(13) Pseudo synchronizing signal (PV/PH) output

(14) Serial interface
- 8-bit clock synchronous mode : 2 channels
- I2C-BUS mode : 1 channel

(15) On-Screen Display (OSD) Control circuit
- 256 characters
- 24 characters x 10 lines

(16) 8-bit A/D Converter : 12 inputs

(17) CTL amplifier, Capstan FG amplifier

(18) Input / Output port : 63 terminals

(19) Interrupt : 18 factors (20 interrupt sources)

(20) Watch dog timer

(21) Operation mode under low Current Consumption (Dual Clock System)
- STOP mode : Oscillation stop (Battery / Capacitor back-up). Port output selection (Data hold / High impedance)
- SLOW mode : Slow speed operation with 32.8 kHz
- IDLE mode : CPU stop / peripheral circuit active at high speed / released by interrupt
- SLEEP mode : CPU stop / peripheral circuit active at slow speed / released by interrupt

(22) The TMP90CR74ADF is molded in a 100-pin Quad Flat Package (QFP100-P-2222A)

Purchase of TOSHIBA I² C components conveys a license under the Philips I² C Patent Rights to use these components in an I² C system, provided that the system conforms to the I² C Standard Specification as defined by Philips.

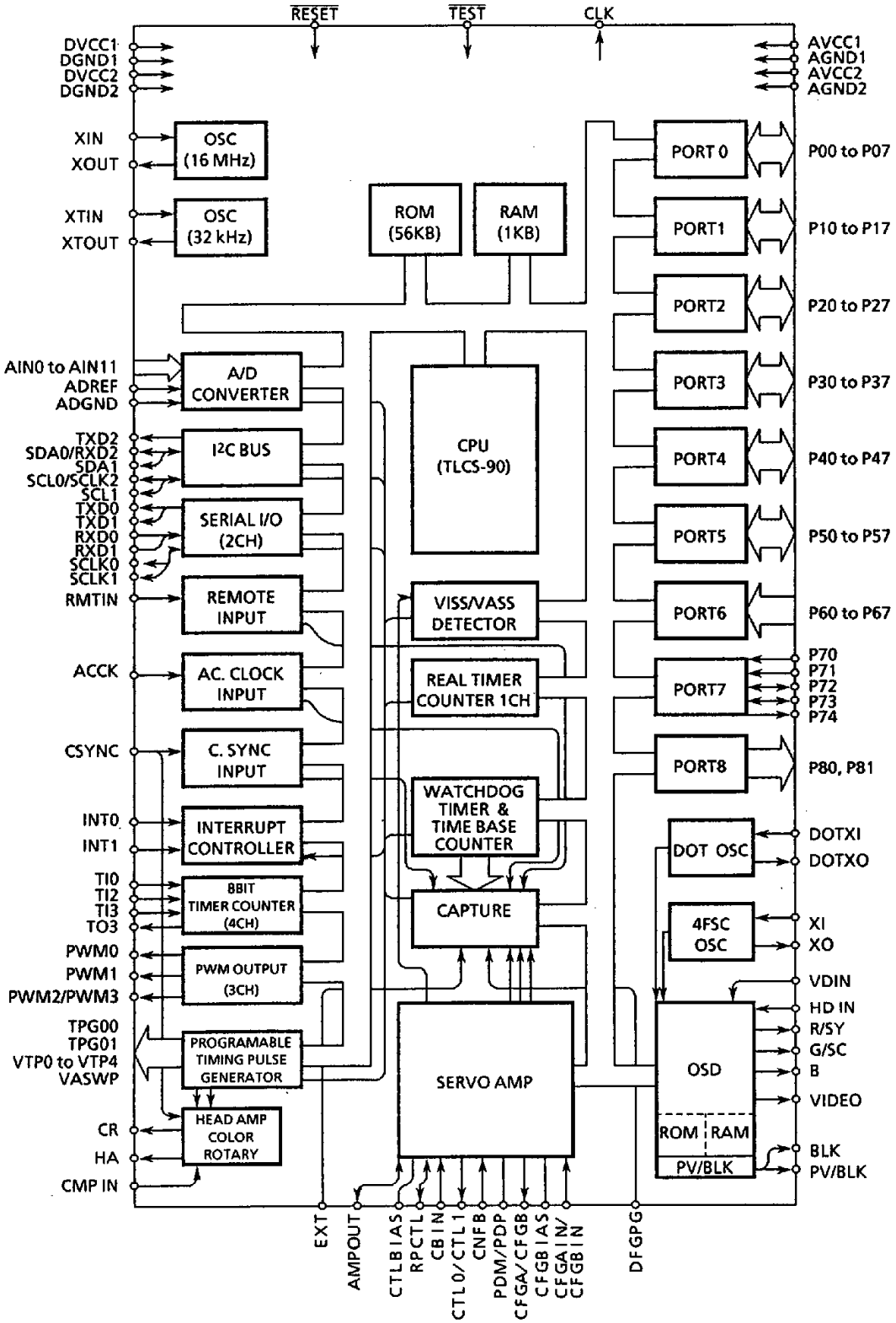


Fig 1.1 TMP90CR74ADF Block Diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The pin assignment of TMP90CR74ADF is shown in Fig. 2.1 and its name and function are in Table 2.1.

2.1 Pin Assignment

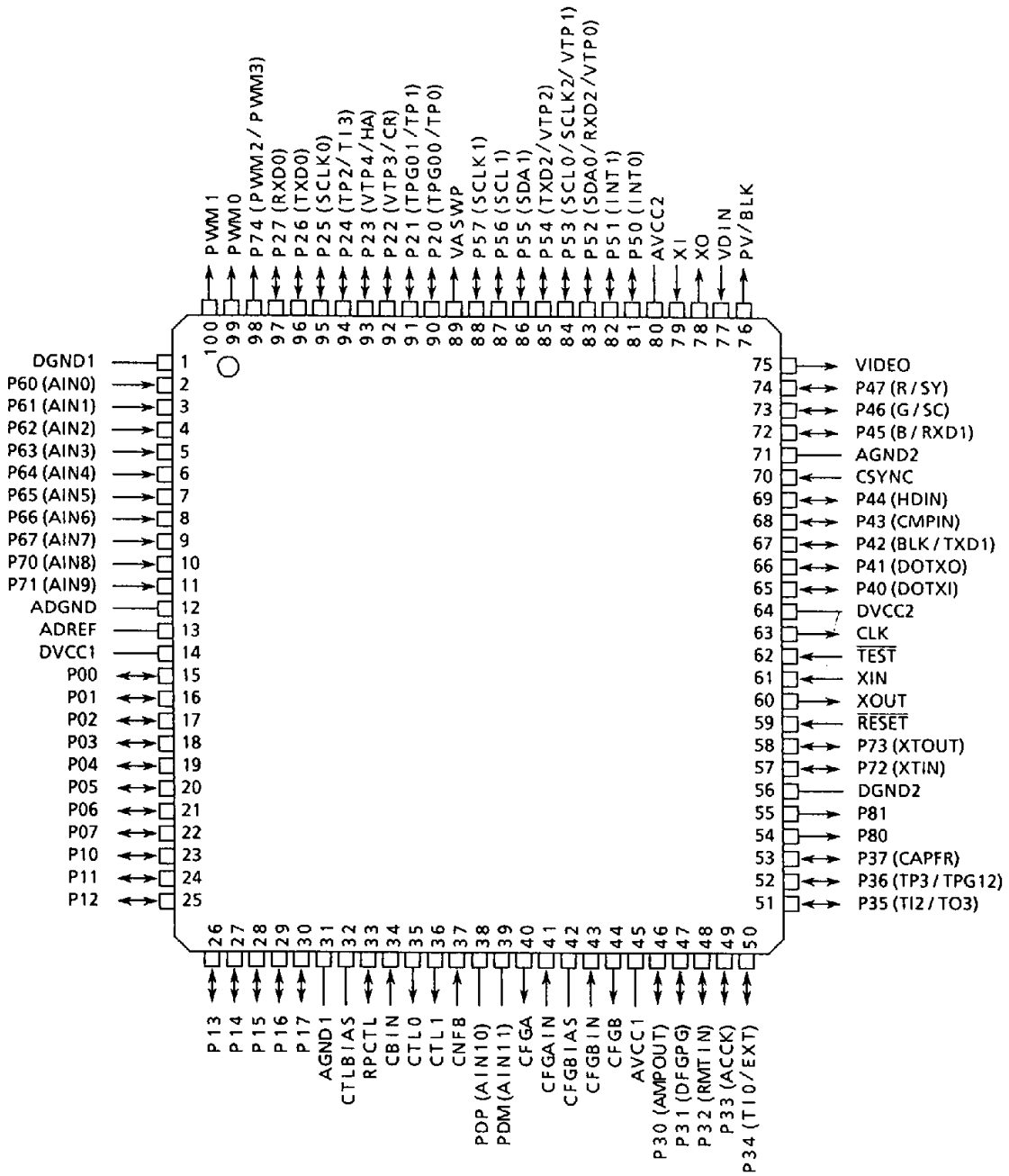


Fig. 2.1 Pin Assignment of TMP90CR74ADF

2.2 Pin name and pin functions

The name and functions of each pin are shown in Table 2.1.

Table 2.1 Pin name and pin functions (1/4)

Pin Name	No. of Pins	I/O Port structure	Function
P00 to P07	8	I/O 3-state	P00 to P07 : 8-bit I/O port. Input and output can be set in bit unit.
P10 to P17	8	I/O 3-state	P10 to P17 : 8-bit I/O port. Input and output can be set in bit unit.
P20 (TPG00 / TP0) P21 (TPG01 / TP1)	2	I/O 3-state Programmable Open Drain	P20, P21 : 2-bit I/O port. Input and output can be set in bit unit. TPG00/TPG01 : Timing Pulse Generator 0 (TPG0) TP0/TP1 : Timing Pulse (TP) output.
P22 (VTP3 / CR) P23 (VTP4 / HA)	2	I/O 3-state Programmable Open Drain	P22, P23 : 2-bit I/O port. Input and output can be set in bit unit. VTP3/VTP4 : Video Timing pulse (VTP) output. CR : Color Rotary output. HA : Head Amp switching signal output.
P24 (TP2 / TI3)	1	I/O 3-state Programmable Open Drain Schmitt input	P24 : 1-bit I/O port. Input and output can be set in bit unit. TP2 : Timing pulse (TP) output. TI3 : Event count input for Timer3 (TC3).
P25 (SCLK0)	1	I/O 3-state Schmitt input	P25 : 1-bit I/O port. Input and output can be set in bit unit. SCLK0 : Serial clock input/output for SIO0.
P26 (TXD0)	1	I/O 3-state	P26 : 1-bit I/O port. Input and output can be set in bit unit. TXD0 : Serial transmit data output for SIO0.
P27 (RXD0)	1	I/O 3-state Schmitt input	P27 : 1-bit I/O port. Input and output can be set in bit unit. RXD0 : Serial receive data input for SIO0.
P30 (AMPOUT)	1	I/O 3-state	P30 : 1-bit I/O port. Input and output can be set in bit unit. AMPOUT : Monitor output of Analog amp (CTL amp / CFG amp) for servo control.
P31 (DFGPG) P32 (RMTIN) P33 (ACCK)	3	I/O 3-state Schmitt input	P31, P32, P33 : 3-bit I/O port. Input and output can be set in bit unit. DFGPG : Input for Drum PG/FG conposite signal. RMTIN : Input for remote control signal. ACCK : Input for AC power frequency.
P34 (TI0 / EXT)	1	I/O 3-state Schmitt input	P34 : I/O port. Input and output can be set in bit unit. TI0 : Event Count input for Timer0 (TC0). EXT : External trigger input for Capture 0 (CAP0).
P35 (TI2 / TO3)	1	I/O 3-state Schmitt input	P35 : 1-bit I/O port. Input and output can be set in bit unit. TI2 : Event Count input for Timer2 (TC2). TO3 : Timer3 (TC3) output.

Table 2.1 Pin name and pin functions (2/4)

Pin Name	No. of Pins	I/O Port structure	Function
P36 (TP3 / TPG12)	1	I/O 3-state Schmitt input	P36 : 1-bit I/O port. Input and output can be set in bit unit. TP3 : Timing pulse (TP) output. TPG12 : Timing pulse generator (TPG1) output.
P37 (CAPFR)	1	I/O 3-state Programmable Open Drain	P37 : 1-bit I/O port. Input and output can be set in bit unit. CAPFR : Capstan motor control output.
P40 (DOTXI) P41 (DOTXO)	2	I/O 3-state	P40, P41 : 2-bit I/O port. Input and output can be set in bit unit. DOTXI / DOTXO : Oscillator terminal for OSD dot-clock.
P42 (BLK / TXD1)	1	I/O Open Drain	P42 : 1-bit I/O port. Input and output can be set in bit unit. BLK : Blanking output for OSD. TXD1 : Serial transmit data output for SIO1.
P43 (CMPIN) P44 (HDIN)	2	I/O 3-state Schmitt input	P43, P44 : 2-bit I/O port. Input and output can be set in bit unit. CMP IN : Comparator signal input for Head Amp switch. HD IN : Horizontal sync. signal input.
P45 (B / RXD1)	1	I/O Open Drain Schmitt input	P45 : 1-bit I/O port. Input and output can be set in bit unit. B : Blue output from OSD. RXD1 : Serial receive data input for SIO1.
P46 (G / SC) P47 (R / SY)	2	I/O 3-state	P46, P47 : 2-bit I/O port. Input and output can be set in bit unit. G, R : Green and Red output from OSD. SC, SY : Chroma, luminance Signal output from OSD.
P50 (INT0) P51 (INT1)	2	I/O 3-state Schmitt input	P50, P51 : 2-bit I/O port. Input and output can be set in bit unit. INT0, INT1 : External interrupt request.
P52 (SDA0/ RXD2/VTP0) P53 (SCL0/ SCLK2/VTP1)	2	I/O 3-state Programmable Open Drain Schmitt input	P52, P53 : 2-bit I/O port. Input and output can be set in bit unit. SDA0 : Serial data I/O for I²CBUS. SCL0 : Serial clock I/O for I²CBUS. RXD2 : Serial receive data input for SIO2. SCLK2 : Serial clock input/output for SIO2. VTP0, VTP1 : Video timing pulse (VTP) output.
P54 (TXD2/ VTP2)	1	I/O 3-state Schmitt input	P54 : 1-bit I/O port. Input and output can be set. TXD2 : Serial transmit data output for SIO2. VTP2 : Video timing pulse (VTP) output.
P55 (SDA1) P56 (SCL1)	2	I/O 3-state Open Drain Schmitt input	P55, P56 : 2-bit I/O port. Input and output can be set in bit unit. SDA1 : Serial data input/output for I²CBUS. SCL1 : Serial clock input/output for I²CBUS.
P57 (SCLK1)	1	I/O Open Drain Schmitt input	P57 : 1-bit I/O port. Input and output can be set. SCLK1 : Serial clock input/output for SIO1.

Table 2.1 Pin name and pin functions (3/4)

Pin Name	No. of Pins	I/O Port structure	Function
P60 (AIN0) to P67 (AIN7) P70 (AIN8) to P71 (AIN9)	10	Input	P60 to P67 : 8-bit input port. P70, P71 : 2-bit input port. AIN0 to AIN9 : Analog input for A/D converter.
P72 (XTIN) P73 (XTOUT)	2	I/O 3-state	P72, P73 : 2-bit I/O port. Input and output can be set in bit unit. XTIN, XTOUT : Oscillator terminals for slow clock (32.768 kHz)
P74 (PWM2 / PWM3)	1	Output 3-state Programmable Open Drain	P74 : 1-bit output port. PWM2/PWM3 : 8-bit / 14-bit PWM (PWM2 / PWM3) output.
P80 P81	2	Output 3-state	P80, P81 : 2-bit output port.
PWM0 PWM1	2	Output 3-state Programmable Open Drain	PWM0 : 12-bit PWM (PWM0) output. PWM1 : 12-bit PWM (PWM1) output.
VASWP	1	Output 3-state	Video / Audio head switching control signal output.
CSYNC	1	Input Schmitt input	Composite sync. signal input.
CTLBIAS	1	–	Bias terminal for control (CTL) amplifier.
RPCTL	1	I/O	Input and output for Control (CTL) signal.
CBIN	1	Input	Bias input terminal for control (CTL) amplifier.
CTL0 CTL1	2	Output	CTL amplifier output for gain switching.
CNFB	1	Input	Negative feed-back terminal of CTL amplifier.
PDP (AIN10)	1		PDP : Terminal for Peak-Hold capacitor which keeps plus (positive) peak for control (CTL) Amplifier. AIN10 : Analog input for PDP level monitor.
PDM (AIN11)	1		PDM : Terminal for Peak-Hold capacitor which keeps plus (positive) peak for control (CTL) Amplifier. AIN11 : Analog input for PDM level monitor.

Table 2.1 Pin name and pin functions (4/4)

Pin Name	No. of Pins	I/O Port structure	Function
CFGA	1	Output	Capstan FG amplifier (CFGA amp.) output.
CFGA IN	1	Input	Capstan FG amplifier (CFGA amp.) input.
CFG BIAS	1	–	Capstan FG amplifier bias terminal.
CFGB IN	1	Input	Capstan FG amplifier (CFGB amp.) input.
CFGB	1	Output	Capstan FG amplifier (CFGB amp.) output.
VIDEO	1	Output	OSD video signal output.
PV / BLK	1	Output 4-state	Pseudo V-SYNC (PV) output / On Screen Display (OSD) Blanking (BLK) output.
VDIN	1	Input Schmitt input	Vertical sync signal input.
XI, XO	2	Input, Output	Oscillator terminals for 4fsc clock of OSD
CLK	1	Output	Clock output : 1/2 or 1/4 of system clock (16 MHz) is output. During RESET operation, output stays high. (Pulled up internally).
$\overline{\text{TEST}}$	1	Input	Test terminal : Should be connected to high.
XIN, XOUT	2	Input, Output	Oscillator terminals for main clock (16 MHz)
$\overline{\text{RESET}}$	1	Input Schmitt input	System reset input.
DVCC1 DVCC2	2	–	Digital Power supply.
DGND1 DGND2	2	–	Digital Ground.
AVCC1 AVCC2	1	–	Analog Power supply.
AGND1 AGND2	1	–	Analog Ground.
ADREF	1	–	A/D converter reference voltage.
ADGND	1	–	A/D converter Ground.

3. OPERATION

This chapter describes the functions and the basic operations of the TMP90CR74A in every block.

3.1 CPU

TMP90CR74A includes a high performance 8 bit CPU. For the function of the CPU, see the previous chapter "TLCS-90 CPU". This chapter explains exclusively the functions of the CPU of TMP90CR74A which are not described in the chapter "TLCS-90 CPU".

3.1.1 Reset

In order to reset the TMP90CR74A, the $\overline{\text{RESET}}$ input must be maintained at the "0" level for at least ten system clock cycles (10 states : 1.25 μs at 16 MHz) within an operating voltage band and with a stable oscillation. When a reset request is accepted, all I/O ports and internal registers are initialized. The registers of the CPU remain unchanged. Note, however, that the program counter PC, the interrupt enable flag IFF are cleared to "0". Register A shows an undefined status.

When the reset is cleared, the CPU starts executing instructions from the address 0000H.

3.1.2 EXF (Exchange Flag)

For TMP90CR74A, "EXF", which is inverted when the instuction "EXX" is executed to transfer data between the main register and the auxiliary register, is allocated to the watch dog timer control register 2 (WDTCR2<EXF> : bit 1 of memory address FFFBH).

WDTCR2 (FFFBH)	7	6	5	4	3	2	1	0
			TBC1F	TBC0F	WDTE		EXF	DRVE

EXF	Exchange Flag	Invert each time EXX instruction is executed.	R

3.2 Memory Map

3.2.1 Internal ROM

The TMP90CR74A contains an 56K-byte ROM. The address space from 0000H to DFFFH is provided to the ROM. The CPU starts executing a program from 0000H by resetting.

The addresses 0008H to 004FH in this internal ROM area are used for the entry area for the interrupt processing.

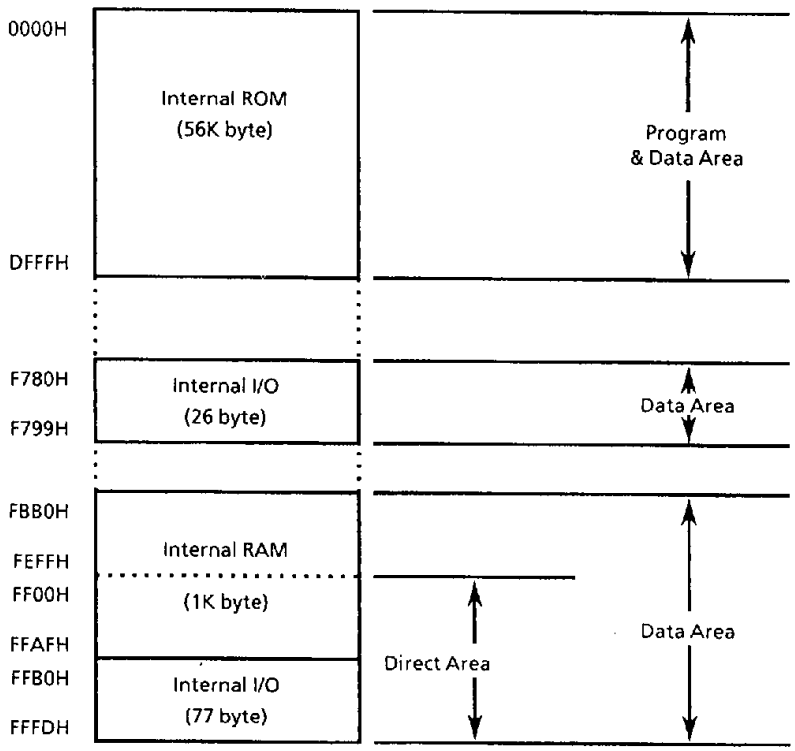
3.2.2 Internal RAM

The TMP90CR74A also contains a 1K-byte RAM, which is allocated to the address space from FBB0H to FFAFH. The CPU allows the access to a certain RAM area (FF00H to FFAFH, 176 bytes) by a short operation code (opcode) in a "direct addressing mode".

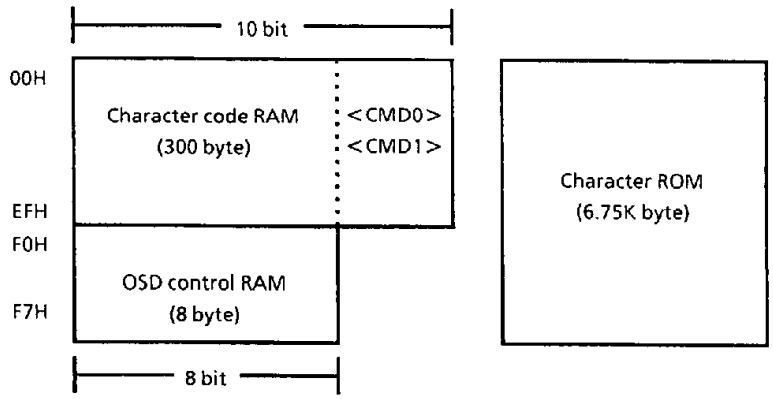
3.2.3 Internal I/O

The TMP90CR74A provides a 103-byte address space as an internal I/O area, whose addresses range from FFB0H to FFFDH (I/O area 1) and F780H to F799H (I/O area 2). This I/O area 1 can be accessed by the CPU using a short opcode in the "direct addressing mode".

Figure 3.2.1 is a memory map indicating the areas accessible by the CPU in the respective addressing mode.



(a) Memory map for CPU



(b) Memory map for OSD control RAM and character ROM

Figure 3.2.1 Memory map

3.3 SYSTEM CLOCK CONTROL

The System Clock Controller consists of Clock Generator, Timing Generator, Standby Controller and Read Time Counter (RTC).

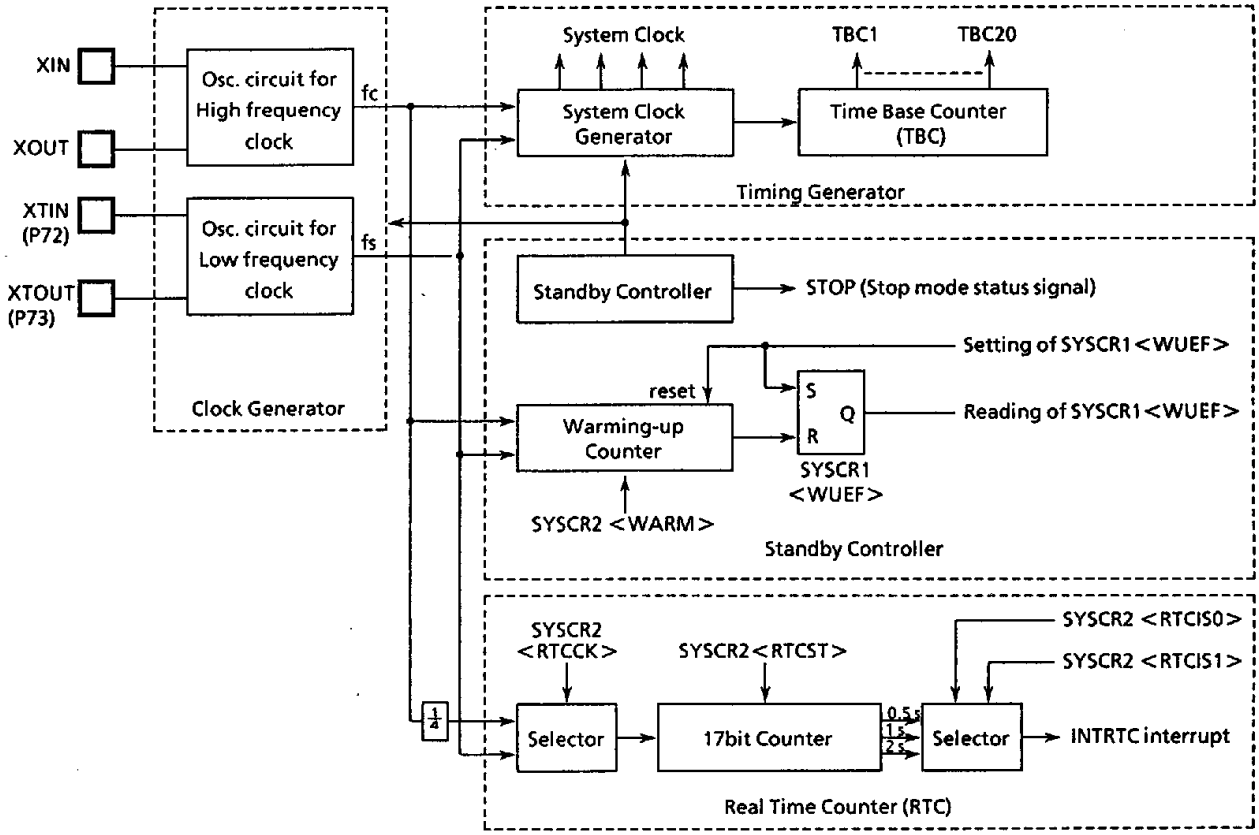


Figure 3.3.1 System Clock Controller

3.3.1 Clock Generator

The Clock Generator is a circuit which generates a basic clock for the system clock; the system clock is provided for CPU and peripheral hardwares. This Clock Generator contains 2 types of oscillating circuit : for high frequency clock and for low frequency clock. Oscillating circuit for the system clock can be selected on Standby Controller, and the current consumption can be reduced by selecting low-speed operation.

High frequency clock (fc) and low frequency clock (fs) are obtained by connecting oscillator between terminals XIN and XOUT and between terminals XTIN and XTOUT respectively. Clock input from external oscillator is also available.

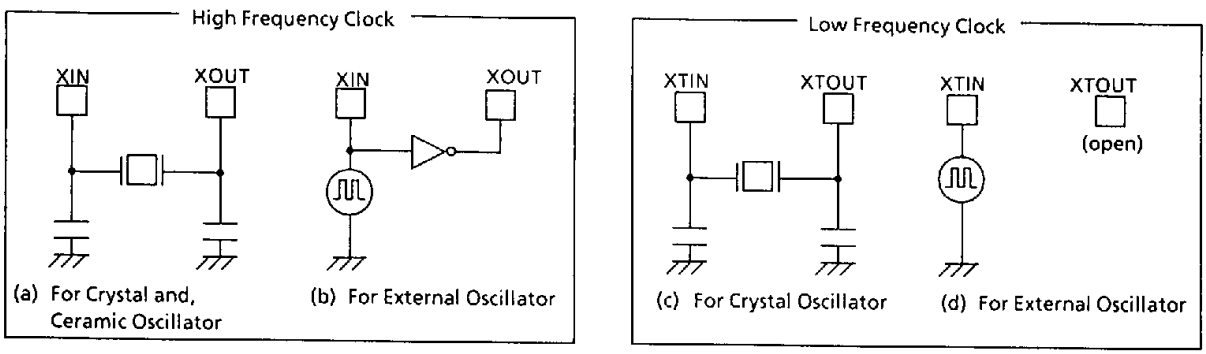


Figure 3.3.2 Connecting Oscillator

3.3.2 Timing Generator

The timing generator generates sorts of system clock from the basic clock (fc or fs), providing for CPU core and peripheral hardwares.

(1) Architecture

The timing generator consists of the system clock generator and the time base counter (TBC) which generates system clock for peripheral hardwares. After resetting, the system clock is generated from high frequency clock (fc) (NORMAL mode). Both Executing the instruction and operating the internal hardwares are synchronized by this system clock.

(2) Time Base Counter

The time base counter consists of a 20-bit up-counter counted by a basic clock divided-by 2 (fc/2 or fs/2), 16-bit data register and control register.

Figure 3.3.3 Shows the structure of the time-base counter (TBC).

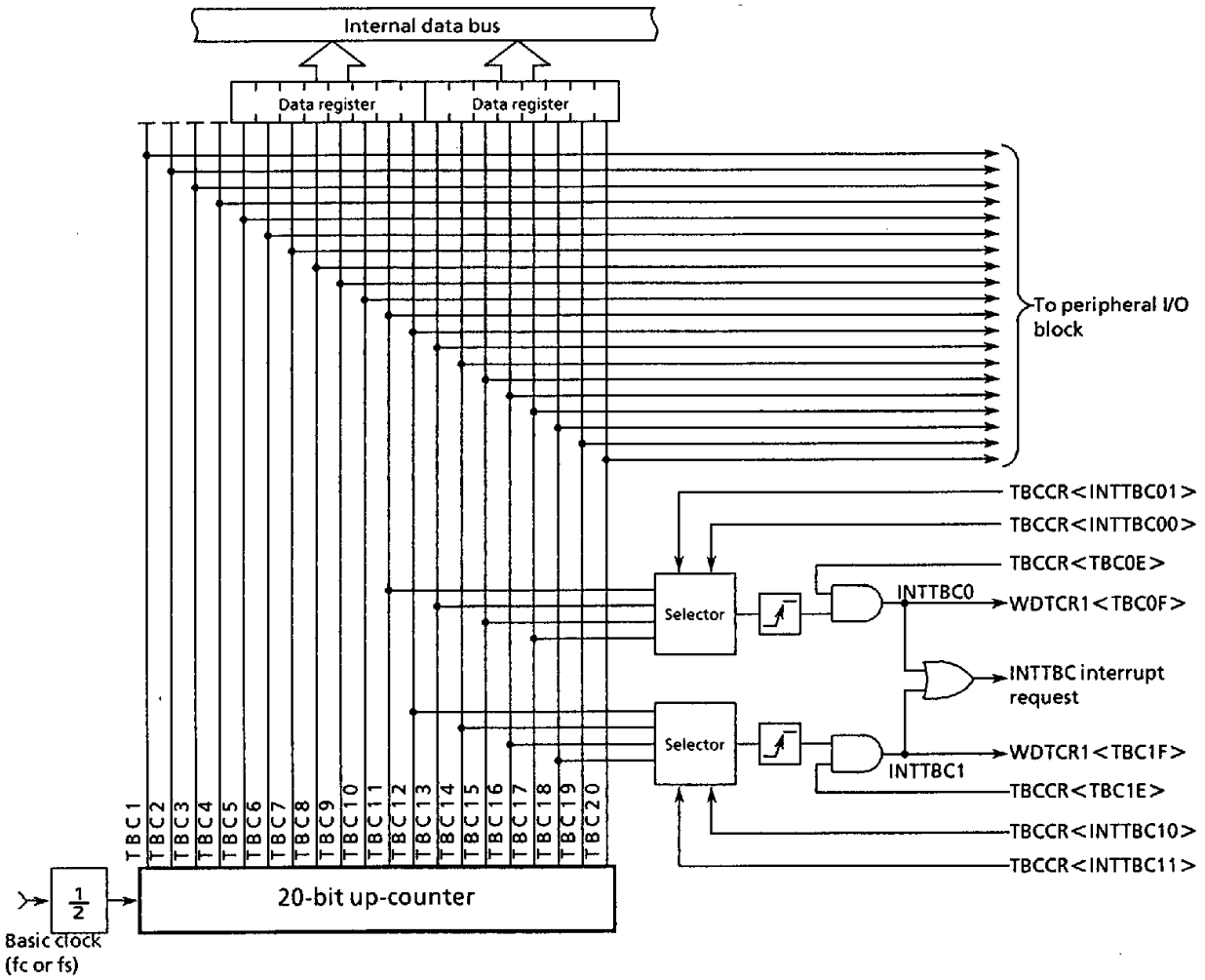


Figure 3.3.3 Structure of Time-Base Counter (TBC)

Time Base Counter Control Register

TBCCR (F798H)

7	6	5	4	3	2	1	0
		TBC1E	TBC0E	INT TBC11	INT TBC10	INT TBC01	INT TBC00

(Reset Value **00 0000)

TBC1E	INTTBC Interrupt Enable / Disable	00 : INTTBC Interrupt Disable 01 : INTTBC0 Interrupt Enable 10 : INTTBC1 Interrupt Enable 11 : INTTBC0 / INTTBC1 Interrupt Enable	R/W
TBC0E			
INTTBC11	INTTBC1 Interrupt Source Clock Selection	00 : TBC12 01 : TBC14 10 : TBC16 11 : TBC18	
INTTBC10			
INTTBC01	INTTBC0 Interrupt Source Clock Selection	00 : TBC11 01 : TBC13 10 : TBC15 11 : TBC17	
INTTBC00			

Time Base Counter Data Register 1

TBCDR1 (FFB2H)

7	6	5	4	3	2	1	0
TBC12	TBC11	TBC10	TBC9	TBC8	TBC7	TBC6	TBC5

(Reset Value 0000 0000) Read only

Time Base Counter Data Register 2

TBCDR2 (FFB3H)

7	6	5	4	3	2	1	0
TBC20	TBC19	TBC18	TBC17	TBC16	TBC15	TBC14	TBC13

(Reset Value 0000 0000) Read only

Watchdog Timer Control Register 1

WDTCR1 (FFFBH)

7	6	5	4	3	2	1	0
		TBC1F	TBC0F	WDTE		EXF	DRVE

TBC1F	INTTBC1 Interrupt Request Flag	0 (W) : Clear 1 (W) : – 0 (R) : No interrupt request 1 (R) : Interrupt request	R/W
TBC0F	INTTBC0 Interrupt Request Flag	0 (W) : Clear 1 (W) : – 0 (R) : No interrupt request 1 (R) : Interrupt request	

① Operation

The time-base counter outputs (TBC1 to TBC20) are used as clock source or timing data for Timer/Counter, Capture (CAP0/CAP1/CAP2), timing pulse generator (TPG), and other peripheral I/O blocks. The contents of time-base counter outputs TBC5 to TBC20 can be read by reading the time-base counter data registers, TBCDR1 and TBCDR2. Note that the data registers must be read in order of TBCDR1 and then TBCDR2.

Time-base counter interrupt requests (INTTBC) can be generated on the rising edges of counter outputs TBC11 to TBC18. The interrupt source is selected by the time-base counter control register TBCCR <INTTBC11, INTTBC10, INTTBC01, and INTTBC00>. The INTTBC interrupt requests are comprised of two interrupt request signals INTTBC0 and INTTBC1 that are logical OR' ed to generate an interrupt request. Which interrupt is requested can be identified by reading the watchdog timer control register 1 WDTCR1 <TBC0F> and <TBC1F>.

The INTTBC0 flag <TBC0F> and INTTBC1 flag <TBC1F> can be cleared by writing "0" in the register.

Table 3.3.1 lists the interval time of time-base counter outputs.

Table 3.3.1 interval time of Time-base Counter (f = fc)

	TBC1	TBC2	TBC3	TBC4	TBC5	TBC6	TBC7	TBC8	TBC9	TBC10
Interval Time [s]	$2^2/f$	$2^3/f$	$2^4/f$	$2^5/f$	$2^6/f$	$2^7/f$	$2^8/f$	$2^9/f$	$2^{10}/f$	$2^{11}/f$
at 16 MHz [μs]	0.25	0.5	1.0	2.0	4.0	8.0	16.0	32.0	64.0	128.0

TBC11	TBC12	TBC13	TBC14	TBC15	TBC16	TBC17	TBC18	TBC19	TBC20
$2^{12}/f$	$2^{13}/f$	$2^{14}/f$	$2^{15}/f$	$2^{16}/f$	$2^{17}/f$	$2^{18}/f$	$2^{19}/f$	$2^{20}/f$	$2^{21}/f$
256.0	512.0	1024	2048	4096	8192	16384	32768	65536	131072

3.3.3 Standby-Controling Circuit

Standby-controling circuit operates for oscillator (high frequency clock, low frequency clock) oscillate/stop and system clock switching. The TMP90CR74A has five operation modes : NORMAL, IDLE, SLOW, SLEEP, and STOP. System control registers (SYSCR1 and SYSCR2) are used to switch between these operation modes. Figure 3.3.4 shows an operation mode transition diagram and the device status in each operation mode.

① NORMAL mode

This mode is to operate CPU core and peripheral hardwares under high frequency clock (fc). The mode after resetting is NORMAL mode (only high frequency clock oscillates).

② IDLE mode

In this mode, the CPU is halted, with the peripheral hardware operated by the high-frequency clock (fc). (Refer to the device status in each operation mode in Figure 3.3.4 (b).) To set IDLE mode, set WDTCR2<HALTM1, HALTM0> to IDLE mode previously, and execute HALT instruction. This IDLE mode is released by interrupt, which comes from peripheral hardwares or external input; afterwards the device becomes NORMAL mode again. When IFF (interrupt enable flag of CPU) is "1" (interrupt is enabled), the device returns to normal operation after the interrupt operation. When IFF is "0" (interrupt is disabled), the device restart from the instruction following HALT for IDLE mode.

③ SLOW mode

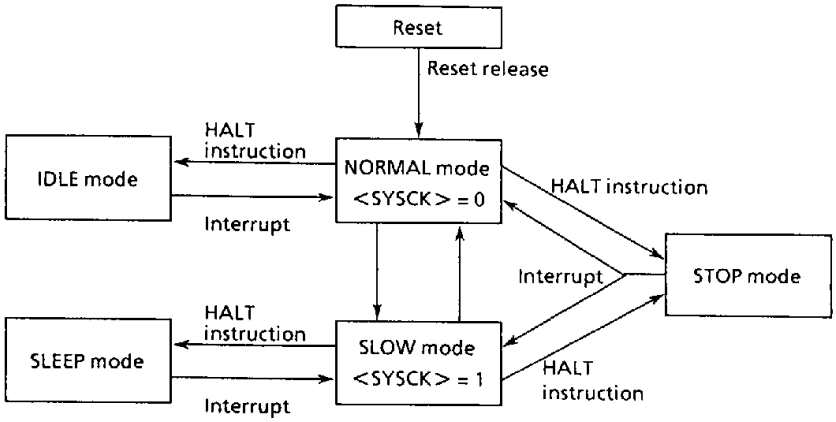
In this mode, the high-frequency clock is made to stop oscillating, with the CPU core and peripheral hardware operated by the low-frequency clock (fs), thus helping to save power consumption greatly. (Refer to the device status in each operation mode in Figure 3.3.4 (b).) Before the SLOW mode is used, the Low-frequency clock (fs) must already be oscillating at the beginning of your application program after the device is cleared of a reset. Switch over from NORMAL to SLOW modes and from SLOW to NORMAL modes are controlled by the system control register <SYSCR1 or SYSCK2>.

④ SLEEP mode

In this mode, the CPU is halted, with the peripheral hardware operated by the low-frequency clock (fs). The same procedure is followed to activate the SLEEP mode and return to the SLOW mode as in the IDLE mode. (Refer to the operation mode transition diagram in Figure 3.3.4 (a).)

⑤ STOP mode

All system operations including oscillating circuit stop under this mode. The device keeps the internal condition under low current consumption. In this case, the I/O port output state can be selected for all ports collectively between output retention or high-impedance state by the watchdog timer control register 1 WDTCR1 <DRVE>. In order to set device to STOP mode, set watchdog timer control register 2 WDTCR2 <HALT1, 0> to STOP mode and execute HALT instruction. Releasing is done by external interrupt INT0 (P50) or INT1 (P51) (Interrupt generation timing is selected either rising edge or falling edge). After the period for warming-up, the device restarts from the instruction followed by HALT instruction when interrupt is disabled. And it restarts after interrupt routine when interrupt is enabled.



(a) Operation Mode Transition Diagram

Operation Mode	Ocsillator		CPU	Peripheral	System Clock
	High freq. (fc)	Lowfreq. (fs)			
RESET	Osc.	Stop	Reset	Reset	High-frequency
NORMAL		Osc. or Stop	Run	Operation	
IDLE			Stop	(Note 1)	
SLOW	Stop	Osc.	Run	(Note 2)	Low-frequency
SLEEP			Stop	(Note 1)	
STOP		Stop		Stop	Stop

(b) Device status in each operation mode

Note 1) The I/O ports retain the previous status immediately before the HALT instruction is executed. The peripheral circuits only (1) time-base counter (TBC), (2) watchdog timer (WDT), (3) real-time counter (RTC), and (4) interrupt control circuit are operating.

Note 2) The operating circuits in this case are (1) I/O ports, (2) time-base counter (TBC), (3) watchdog timer (WDT), (4) real-time counter (RTC), and (5) interrupt control circuit. (All other peripheral circuits and their interrupts must be disabled before they are placed in the SLOW mode.)

Figure 3.3.4 Operation mode transition diagram and device status

System Control Resister 1

SYSCR1 (FFB0H)

7	6	5	4	3	2	1	0
	SYSCK	XEN	XTEN	RXEN	RXTEN	RSYSCK	WUEF

(Reset Value *010 1000)

SYSCK	(W) System Clock Mode Select (R) Monitor	0 : High Frequency Clock Mode 1 : Low Frequency Clock Mode	R/W
XEN	(W) High Frequency Oscillator Control (R) Monitor	0 : Stop Oscillation 1 : Continue / Restart Oscillation	
XTEN	(W) Low Frequency Oscillator Control (R) Monitor	0 : Stop Oscillation 1 : Continue / Restart Oscillation	
RXEN	High Frequency Oscillator Control after restarting from Stop mode	0 : Stop Oscillation 1 : Restart Oscillation	
RXTEN	Low Frequency Oscillator Control after restarting from Stop mode	0 : Stop Oscillation 1 : Restart Oscillation	
RSYSCK	System Clock Mode Select after restarting from STOP mode	0 : High Frequency Clock Mode 1 : Low Frequency Clock Mode	
WUEF	(W) Warming-up Counter Control (R) Warming-up flag (Monitor)	0 : (W) – (R) Warming-up Complete 1 : (W) Warming-up Start, (R) In Warming-up	

System Control Resister 2

SYSCR2 (FFB1H)

7	6	5	4	3	2	1	0
			RTCCK	RTCST	RTCIS1	RTCIS0	WARM

(Reset Value ***0 0000)

RTCCK	RTC Clock Source Select	0 : Low Frequency Clock 1 : High Frequency Clock	R/W
RTCST	RTC Start Control	0 : Stop and Counter Clear 1 : Start	
RTCIS1 RTCIS0	Interval Time Control of RTC Interrupt	00 : fc/2^{15} or fs/2^{15} (1.0) [s] 01 : fc/2^{16} or fs/2^{16} (2.0) [s] 10 : fc/2^{14} or fs/2^{14} (0.5) [s] 11 : Inhibited	
WARM	Warming-up Time Select	0 : 2^{14}/fc or 2^{14}/fs [s] 1 : 2^{16}/fc or 2^{16}/fs [s]	

Watchdog Timer Control Register 1

WDTCR1 (FFFBH)

7	6	5	4	3	2	1	0
		TBC1F	TBC0F	WDTE		EXF	DRVE

(Reset Value **00 0*00)

DRVE	Controlling output status for port during STOP mode	0 : High Impedance 1 : Keep the status throughout setting STOP mode	R/W

Watchdog Timer Control Register 2

WDTCR1 (F797H)

7	6	5	4	3	2	1	0
				WDTP1	WDTP0	HALTM1	HALTM0

(Reset Value **** 0000)

HALTM1 HALTM0	Setting Stand-by mode	00 : – 01 : STOP mode 10 : IDLE mode or SLEEP mode 11 : don't use	R/W

3.3.4 Controlling Operation Mode

(1) STOP mode

STOP mode is to be set by executing HALT instruction when watchdog timer control register 2 WDTCR2 <HALT1, 0> = "01". During STOP mode, both high frequency and low frequency stop oscillation and all operations are stopped. Data memory, registers, output laches for ports keep the status of just before the HALT instruction. The output for ports is selected whether to keep output or to be high impedance by setting <DRVE> in watchdog timer control register 1 (WDTCR1).

Releasing STOP mode is done by interrupt or resetting. If CPU is EI (interrupt master enable flag IFF is "1"), the interrupt is accepted and CPU starts interrupt processing. If CPU is DI (interrupt enable flag IFF is "0"), CPU restart from the instruction followed by HALT; in this case, the interrupt request flag for releasing is required to be cleared after releasing.

If STOP mode is released by resetting (RESET terminal to "L" level), even though the register setting for returned mode is SLOW mode, the device restarts from NORMAL mode.

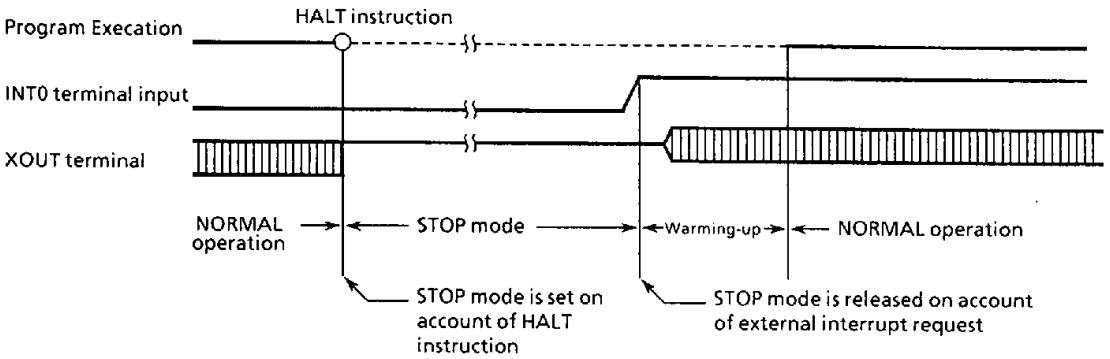


Figure 3.3.5 Sequence example for STOP mode

STOP mode is released by following sequence.

① The oscillation starts. By setting system control register 1 SYSCR1 <RXEN, RXTEN, RSYSCK>, the operation mode after the STOP mode can be selected; setting the register <RXEN, RXTEN, RSYSCK> should precede HALT instruction for STOP mode.

Table 3.3.2 Operation Mode Setting after Exiting STOP Mode

	<RXEN>	<RXTEN>	<RSYSCK>
Recovering to NORMAL mode	1	0	0
Recovering to SLOW mode	0	1	1

Note 1) If an interrupt request for releasing STOP mode occur when the "HALT" instruction is executed, the operation mode which is determined by SYSCR1<SYSCK, XEN, XTEN> at the execution of HALT instruction will be maintained.

Note2) The operation mode can be confirmed by reading system control register SYSCR1 <SYSCK, XEN, XTEN>.

② Warming-up is executed in order to keep time waiting for stabilizing oscillation. During warming-up, the internal operation is still stopping. Time length for warming-up can be selected from 2 on system control register 2 SYSCR2 <WARM> to fit an oscillation characteristics.

The clock source for warming-up counter is selected by hardware; high frequency clock (fc) is to recover NORMAL mode and low frequency clock (fs) is to recover SLOW mode.

Table 3.3.3 Warming-up Time (When Exiting STOP Mode)

<WARM>	To operate in NORMAL mode (@ fc = 16 [MHz])	To operate in SLOW mode (@ fs = 32.768 [kHz])
0	1.024 ms	500 ms
1	4.096 ms	2 s

③ After warming-up time is completed, normal operation (NORMAL mode or SLOW mode) is restarted.

(2) IDLE (SLEEP) mode

The IDLE (SLEEP) mode is entered by executing a HALT instruction after setting the watchdog timer control register 2 (WDTCR2) <HALTM1, HALTM0> to '10'. In this mode, the CPU stops operating, with part of the peripheral circuits continuing operation. (Refer to the device status in each operation mode in Figure 3.3.4 (b).)

The IDLE (SLEEP) mode is released by an interrupt request or a reset (with the RESET pin pulled low). If a non-maskable interrupt or a maskable interrupt is in EI state, an interrupt routine will be executed after releasing from the IDLE (SLEEP) mode. If the interrupt is in DI state, an instruction next to the HALT will be executed after releasing from the IDLE (SLEEP) mode. The interrupt requeset flag which is used as a mode releasing signal should be cleared to "0".

The interrupt source that can be used to release the IDLE (SLEEP) mode is (1) watchdog timer interrupt (INTWDT), (2) timebase counter interrupt (INTTBC), (3) realtime counter interrupt (INTRTC), (4) external interrupt (INT0), or (5) external interrupt (INT1).

If the device is reset when in IDLE (SLEEP) mode, the device starts up from the NORMAL mode.

(3) SLOW mode

The SLOW mode is controlled by system control register 1, 2 (SYSCR1, 2) and warming-up counter.

① Switch over from NORMAL to SLOW mode

First, set the SYSCR1 <XTEN> to "1" to activate the low-frequency clock (fs). After the oscillation stabilizes, set the SYSCR1 <SYSCK> to "1" to switch over the system clock to the low-frequency clock (fs) (The low-frequency clock (fs) had better been already oscillating at the beginning of application program). Then reset the SYSCR1 <XEN> to "0" to stop the high-frequency oscillator.

It may be convenient to use the warming-up counter to confirm the stabilized low-frequency clock (fs). The warming-up counter starts counting the low-frequency clock (fs) by setting the SYSCR1 <WUEF> to "1". The <WUEF> bit is cleared to "0" after an elapse of the warming-up time that is set in the SYSCR2 <WARM>.

Table 3.3.4 shows the warming-up time at which the mode is switched over from NORMAL to SLOW.

Table 3.3.4 Warming-up time (for shifting from NORMAL to SLOW mode)

<WARM>	@ fs = 32.768 [kHz]
0	500 ms
1	2 s

Note 1) The warming-up time is derived by dividing the low-frequency clock (fs) by the warming-up counter. For this reason, the warming-up time includes an error, because of the unstable oscillation at the start-up. Therefore, the warming-up time must be handled as an approximate value.

Note 2) If the low-frequency clock (fs) does not have its oscillation stabilized even when the warming-up flag <WUEF> is cleared to "0", perform warming-up operation several times until the oscillation stabilizes.

Figure 3.3.6 shows a switching over sequence from NOMAL to SLOW mode.

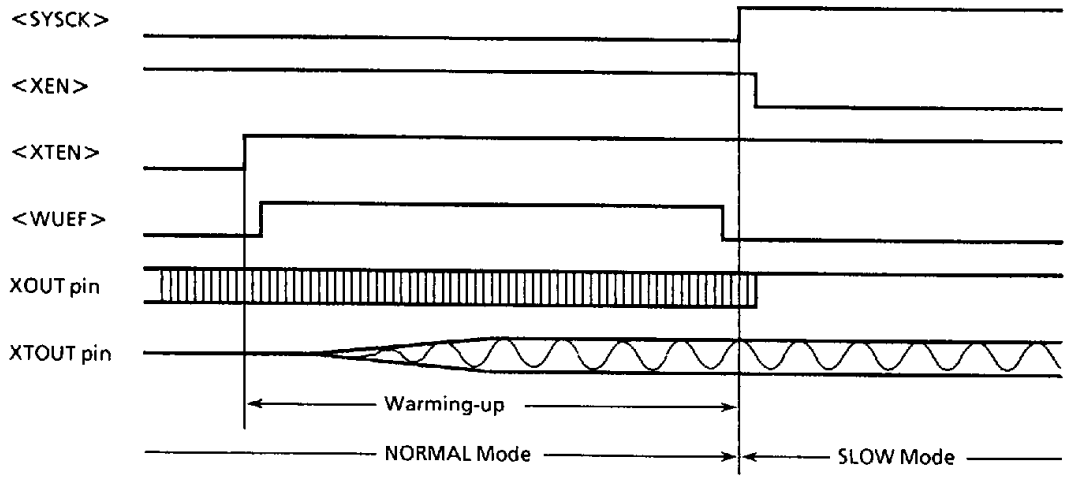


Figure 3.3.6 Switching over sequence from NORMAL to SLOW mode

② Switch over from SLOW to NORMAL mode

First, set the SYSCR1 <XEN> to "1" to acrivate the high-frequency clock (fc) to start oscillating. After waiting for the oscillation to stabilize, reset the SYSCR1 <SYSCK> to "0" to switch the system clock from the low-frequency to the high-frequency clock (fc).

It may be convenient to use the warming-up counter to confirm the stabilized high-frequency clock (fc). The warming-up counter starts counting the high-frequency clock (fc) by setting the SYSCR1 <WUEF> to "1". The <WUEF> is cleared to "0" after an elapse of the warming-up time that is set in the SYSCR2 <WARM>.

Table 3.3.5 shows the warming-up time at which the mode is switched over from SLOW to NORMAL.

Table 3.3.5 Warming-up time (for shifting from SLOW to NORMAL mode)

<WARM>	@ fc = 16 [MHz]
0	1.024 ms
1	4.096 ms

Note 1) The warming-up time is derived by dividing the high-frequency clock (fc) by the warming-up counter. For this reason, the warming-up time includes an error, because of the unstable oscillation at the start-up. Therefore, the warming-up time must be handled as an approximate value.

Note 2) If the high-frequency clock (fc) does not have its oscillation stabilized even when the warming-up flag <WUEF> is cleared to "0", perform warming-up operation several times until the oscillation stabilizes.

Figure 3.3.7 shows a switching over sequence from SLOW to NORMAL mode.

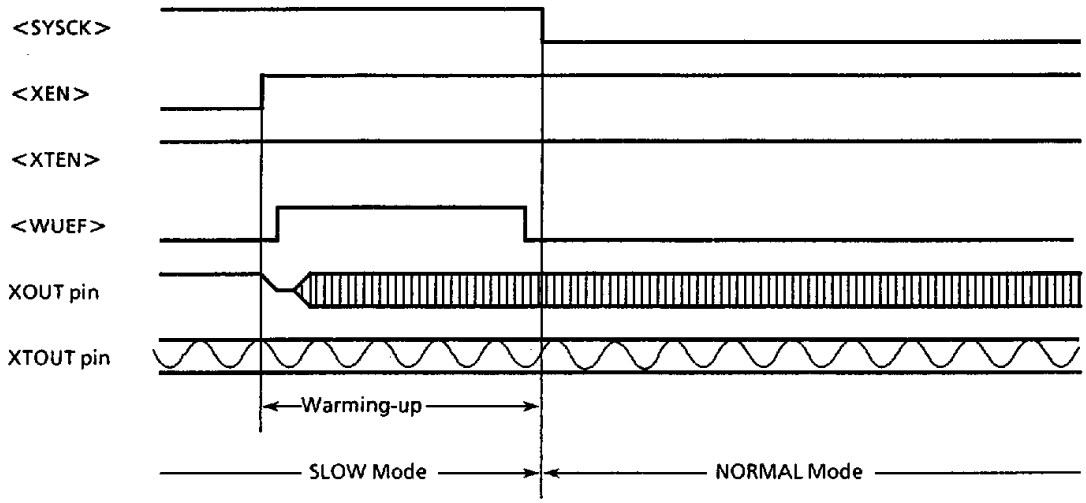


Figure 3.3.7 Switching over sequence from SLOW to NORMAL mode

3.3.5 Real Time Counter (RTC)

The TMP90CR74A has the real time counter (RTC) which generates a periodic interrupt request. The RTC is controlled by System Control Register2 (SYSCR2).

The RTC is a 17bit binary counter and its clock source is selected either low frequency clock (fs) or high frequency clock (fc/4). To start/stop the counter is controlled by <RTCST>.

The period of interrupt request INTRTC is selected from 3 types by setting <RTCIS1, RTCIS0>.

Table 3.3.6 shows the period of interrupt request INTRTC.

Table 3.3.6 INTRTC Interrupt Interval

<RTCCK>	<RTCIS 1, 0>	INTRTC interrupt interval
0 (fs = 32.768 kHz)	00	1 s
	01	2 s
	10	0.5 s
1 (fc = 16 MHz)	00	8.192 ms
	01	16.384 ms
	10	4.196 ms

3.4 INTERRUPT CONTROLLER

The TMP90CR74A has 18 types (external : 2, internal : 16) of interrupt factors (As a source, 2 types for external and 18 types for internal; totaled 20). Two of internal are non-maskable and others are maskable.

The interrupt factor has own interrupt request flag (IRF) to keep the request for interrupt; every interrupt request flag has a vector independently. Interrupt request flag is set to "1" on occurring of interrupt request and requires acceptance for interrupt to CPU.

The acceptance for each interrupt can be enable independently by interrupt enable flag (IFF) and Interrupt Enable register (INTE). If the plural interrupt are generated simultaneously, the interrupt with higher priority is accepted first; the priority is fixed on hardware.

Table 3.4.1 Interrupt Sources

Priority		Interrupt Sources	Type	Clear Code for Interrupt	Vector address
Highest	1	INTSWI (Software Interrupt)	Non Maskable	—	0008H
	2	INTWDT (Watchdog Timer)		—	000CH
	3	INT0 (External input 0)	Maskable	04H	0010H
	4	INTCAP1 (Capture 1)		05H	0014H
	5	INTCAP0 (Capture 0)		06H	0018H
	6	INTTPG0 (Timing Pulse Generator 0)		07H	001CH
	7	INTTPG1 (Timing Pulse Generator 1)		08H	0020H
	8	INTIIC (I^2CBus)		09H	0024H
	9	INTTBC (Time Base Counter)		0AH	0028H
	10	INTT0 (Timer Counter 0)		0BH	002CH
		INTDIR (Capstan invert detection)			
	11	INTSIO0 (Serial Interface 0)		0CH	0030H
	12	INTSIO1 (Serial Interface 1)		0DH	0034H
	13	INTT1 (Timer Counter 1)		0EH	0038H
	14	INTT2 (Timer Counter 2)		0FH	003CH
	15	INTT3 (Timer Counter 3)		10H	0040H
		INTAD (A/D conversion)			
	16	INTVA (VISS/VASS detection)		11H	0044H
	17	INT1 (External input 1)		12H	0048H
Lowest	18	INTRTC (Real Time Counter)		13H	004CH

When an interrupt is requested by software or from internal I/O block the interrupt request is transferred to the CPU via an interrupt controller. The CPU starts the interrupt processing if it is a non-maskable or maskable interrupt requested in the EI state (Interrupt enable flag (IFF) = "1"). However , a maskable interrupt requested in the DI state (IFF = "0") is ignored.

Having acknowledged an interrupt, the CPU reads out the interrupt vector from the interrupt controller and jumps to an interrupt routine.

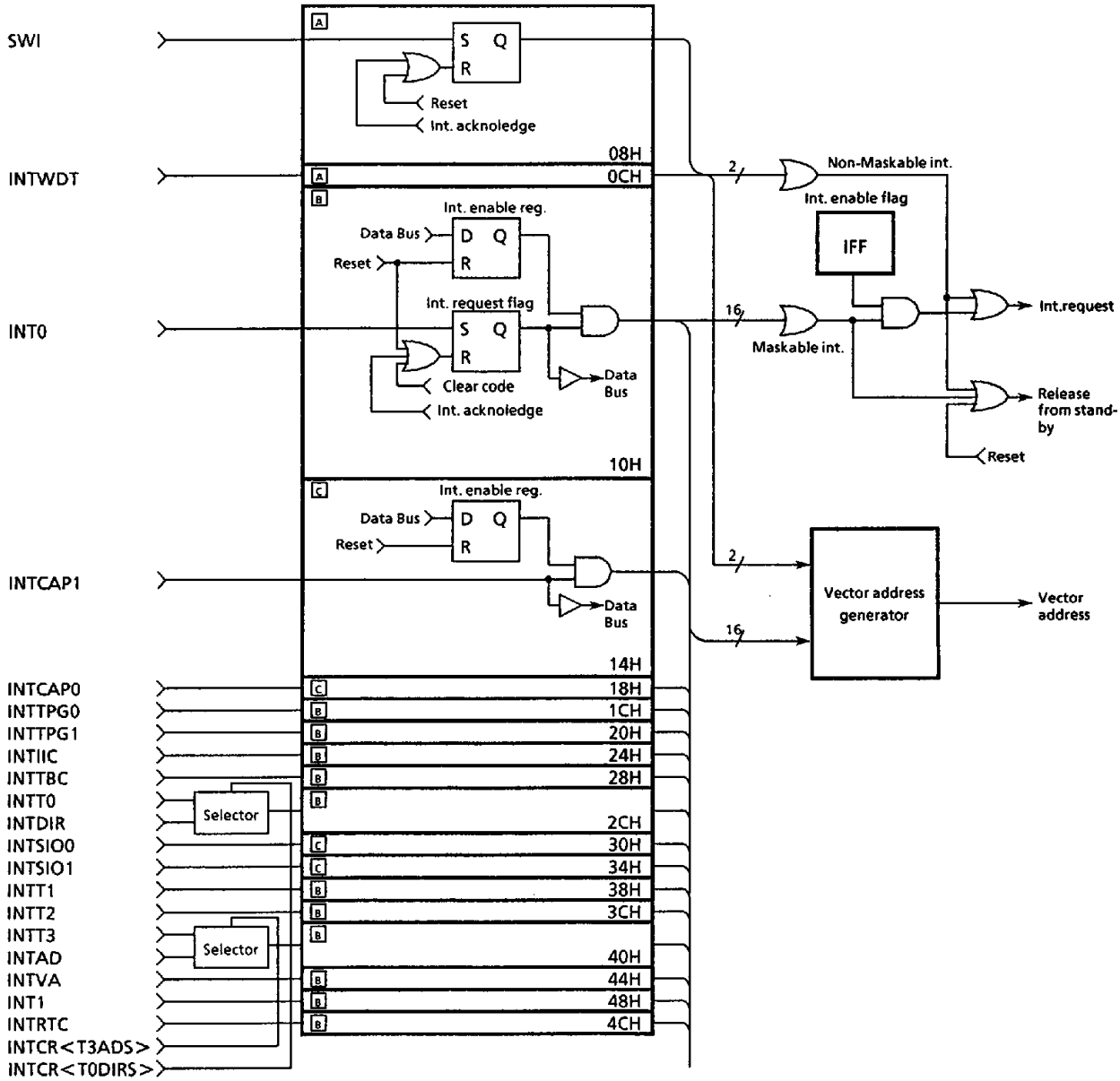


Figure 3.4.1 Configuration of Interrupt Controller

3.4.1 Interrupt processing

A non-maskable interrupt can't be disabled by programming. A maskable interrupt, on the other hand, can be enabled or disabled by programming.

An interrupt enable flag (IFF) is assigned on the bit 5 of Register F in the CPU. The interrupt is enabled or disabled by setting IFF to "1" by the EI instruction or to "0" by the DI instruction, respectively. IFF is reset to "0" by the Reset operation or the acceptance of interrupt. The interrupt can be enabled after the subsequent instruction of EI instruction is executed.

Fig. 3.4.2 shows an interrupt processing flowchart.

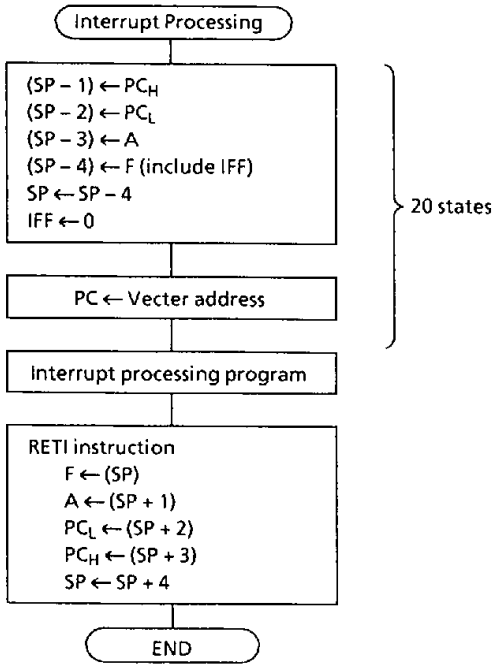


Figure 3.4.2 Interrupt Processing Flowchart

The CPU stores the contents of program counter (PC) and the register pair AF (including the interrupt enable flag (IFF) before the accepting interrupt) into the stack, and resets the interrupt enable flag (IFF) to "0" (disable interrupts). Then, an interrupt controller transfers the interrupt vector to the program counter, and the program jumps to the interrupt routine. When vector has been read out, interrupt request flag (IRF) is cleared to "0".

The overhead from accepting an interrupt to jumping to an interrupt routine is 20 states (2.5 μs at fc = 16 MHz).

An interrupt (Maskable and Non-maskable) routine is completed by a RETI instruction. When the RETI instruction is executed, the data previously stacked from the program counter (PC) and the register pair (AF) are restored. Then, the interrupt enable flag (IFF) returns to the state before the interrupt.

3.4.2 Interrupt Controller

The "priority" in the Table3.4.1 means the order of the interrupt source to be acknowledged by the CPU when plural interrupts are requested at the same time. If interrupts of 3rd and 4th priorities are requested simultaneously, for example, CPU accepts an interrupt of 3rd priority, first. After the 3rd priority interrupt processing has been completed by a RETI instruction, the CPU accepts an interrupt of 4th priority. If an EI instruction is executing in the 3rd priority interrupt routine, then the 4th priority interrupt is accepted.

The interrupt controller merely determines the priority of the sources of interrupts to be accepted by the CPU when plural interrupts are requested at the same time. It is, therefore, unable to compare the priority of interrupt being executed with the one being requested. In order to permit another interrupt during a certain interrupt routine, set the interrupt enable register (INTE1/INTE2) for the interrupt to be allowed and execute the EI instruction.

Fig.3.4.1 shows a configuration of the interrupt controller. The interrupt controller consists of Interrupt Request Flag (IRF) and Interrupt Enable register (INTE) allocated to each of interrupt channels. The interrupt request flag (IRF) is a flip-flop to maintain an interrupt request from internal I/O. Each flip-flop is reset to "0" by resetting or reading out the vector by CPU when an interrupt is accepted. The interrupt request flag (IRF) can be reset by an instruction which write clear code (Refer to Table 3.4.1) to the address F790 (H).

Example) In case of resetting the interrupt request flag of INT0 (External interrupt 0), write the clear code "04 (H)" to the address F790 (H).

```
LD    (F790H), 04H
```

The state of interrupt request flag (IRF) can be checked by reading the address F790(H) for IRF1 and F791(H) for IRF2.

Caution) The clear code must be written in DI state.

Note) Following 4 interrupt sources in 16 maskable interrupts don't have interrupt request flag. Refer to the explanation of individual I/O function about clearing the interrupt request.

INTCAP0 : Interrupt from Capture 0
INTCAP1 : Interrupt from Capture 1
INTSIO0 : Interrupt from SIO 0
INTSIO1 : Interrupt from SIO 1

The Interrupt Enable registers (INTE) are assigned to the address F78D (H):INTE1 and F78E (H):INTE2. Setting any of these bits to "1" enables an interrupt of the respective channel and "0" disables an interrupt. These bits are initialized to "0" by resetting.

3.4.3 Interrupt Control Register

Followings are bit function of Interrupt Request Flag (IRF1, IRF2), Interrupt Enable Register (INTE1, INTE2) and Interrupt Control Register (INTCR).

Interrupt Request Flag 1

IRF1 (F790H)

7	6	5	4	3	2	1	0
IRFT0DIR	IRFTBC	IRFIIC	IRFTPG1	IRFTPG0	IRFCAP0	IRFCAP1	IRF0

(Initial Value 0000 0000)

IRFT0DIR	INTT0DIR Interrupt Request Flag	0 : No Interrupt Request 1 : Interrupt Request	R/W
IRFTBC	INTTBC Interrupt Request Flag		
IRFIIC	INTIIC Interrupt Request Flag		
IRFTPG1	INTTPG1 Interrupt Request Flag		
IRFTPG0	INTTPG0 Interrupt Request Flag		
IRFCAP0	INTCAP0 Interrupt Request Flag		
IRFCAP1	INTCAP1 Interrupt Request Flag		
IRF0	INT0 Interrupt Request Flag		

Interrupt Request Flag 2

IRF2 (F791H)

7	6	5	4	3	2	1	0
IRFRTC	IRF1	IRFVA	IRFT3AD	IRFT2	IRFT1	IRFSIO1	IRFSIO0

(Initial Value 0000 0000)

IRFRTC	INTRTC Interrupt Request Flag	0 : No Interrupt Request 1 : Interrupt Request	read only
IRF1	INT1 Interrupt Request Flag		
IRFVA	INTVA Interrupt Request Flag		
IRFT3AD	INTT3AD Interrupt Request Flag		
IRFT2	INTT2 Interrupt Request Flag		
IRFT1	INTT1 Interrupt Request Flag		
IRFSIO1	INTSIO1 Interrupt Request Flag		
IRFSIO0	INTSIO0 Interrupt Request Flag		

Interrupt Enable Register 1

INTE1 (F78DH)

7	6	5	4	3	2	1	0
IET0DIR	IETBC	IEIIC	IETPG1	IETPG0	IECAP0	IECAP1	IE0

(Initial Value 0000 0000)

IET0DIR	INTT0DIR Interrupt Enable / Disable	0 : Disable 1 : Enable	R/W
IETBC	INTTBC Interrupt Enable / Disable		
IEIIC	INTIIC Interrupt Enable / Disable		
IETPG1	INTTPG1 Interrupt Enable / Disable		
IETPG0	INTTPG0 Interrupt Enable / Disable		
IECAP0	INTCAP0 Interrupt Enable / Disable		
IECAP1	INTCAP1 Interrupt Enable / Disable		
IE0	INT0 Interrupt Enable / Disable		

Interrupt Enable Register 2

INTE2 (F78EH)

7	6	5	4	3	2	1	0
IERTC	IE1	IEVA	IET3AD	IET2	IET1	IESIO1	IESIO0

(Initial Value 0000 0000)

IERTC	INTRTC Interrupt Enable / Disable	0 : Disable 1 : Enable	R/W
IE1	INT1 Interrupt Enable / Disable		
IEVA	INTVA Interrupt Enable / Disable		
IET3AD	INTT3AD Interrupt Enable / Disable		
IET2	INTT2 Interrupt Enable / Disable		
IET1	INTT1 Interrupt Enable / Disable		
IESIO1	INTSIO1 Interrupt Enable / Disable		
IESIO0	INTSIO0 Interrupt Enable / Disable		

Interrupt Control Register

INTCR (F78FH)

7	6	5	4	3	2	1	0
		CLKCK	$\overline{\text{CLOE}}$	INT TPG0E	INT TPG0S	T3ADS	T0DIRS

(Initial value **00 0000)

INTTPG0E	Edge selection of INTTPG0 edge (Interrupt source: TPG03)	0 : TPG03 leading edge 1 : TPG03 trailing edge	R/W
INTTPG0S	Selection of INTTPG0 interrupt source	0 : FIFO buffer empty interrupt 1 : FIFO buffer empty/TPG03 interrupt	
T3ADS	Selection of INTT3AD interrupt source	0 : INTT3 interrupt 1 : INTAD interrupt	
T0DIRS	Selection of INTT0DIR interrupt source	0 : INTT0 interrupt 1 : INTDIR interrupt	

Note 1) Clearing the interrupt request flag should be done in the DI state.

2) Only clear code can be written into Interrupt request flag 1 (IRF1).
When clearing the interrupt request located on Interrupt request flag 2 (IRF2), its clear code should be written into Interrupt flag 1 (IRF1 : address F790H).

3) Since the interrupt request from INTCAP0, INTCAP1, INTSIO0 and INTSIO1 comes in level signal to the interrupt controller, the interrupt request flags can not be cleared even if the interrupt request clearing vector is written to F790H.

4) Two interrupt requests are shared by two sources between INTT0 and INTDIR, between INTT3 and INTAD. After reset operation, INTT0 and INTT3 are selected as interrupt request sources. The sources can be changed by setting INTCR<T0DIRS> and INTCR<T3ADS> bits to "1".

3.4.4 External interrupt input

The TMP90CR74A has 2 channels of external interrupt inputs (INT0,INT1). The INT0 input is assigned to P50 terminal and INT1 is assigned to P51. The interrupt timing of rising edge or falling edge for INT0/INT1 can be selected by setting of P5 mode register (P5MR<INTE0> and <INTE1>) which address is F787 (H).

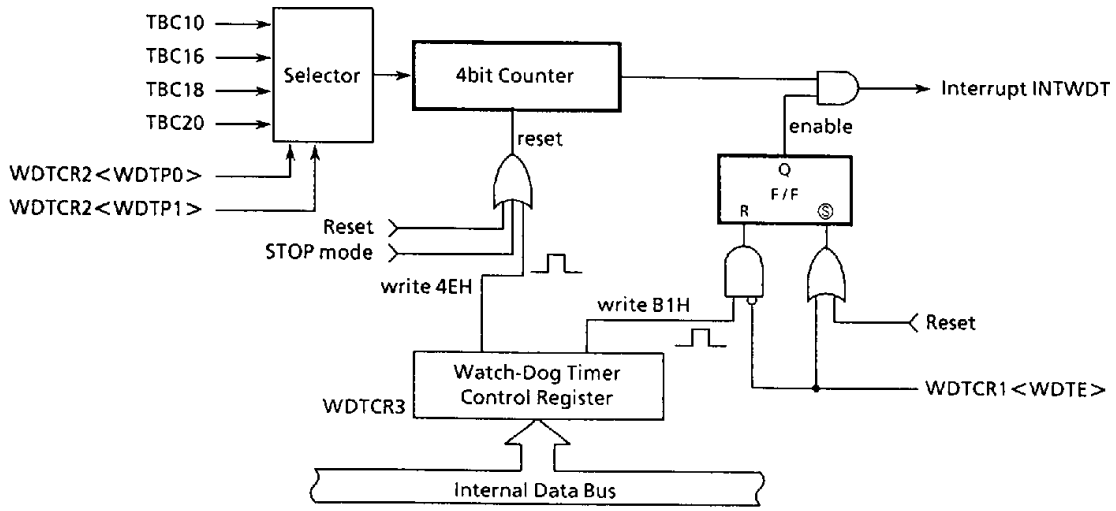
A minimum pulse width for accepting interrupt of INT0 and INT1 is 22/fc (250 ns at fc = 16 MHz) or 22/fs (125 μs at fs = 32 kHz) for both "High" and "Low" level pulse width.

3.5 WATCHDOG TIMER (WDT)

If noise or other factors cause the CPU to operate in error (malfunction), the watchdog timer (WDT) detects that fact so that the CPU can be returned to normal operating condition. When the WDT detects malfunction, a non-maskable interrupt is generated to tell the CPU.

3.5.1 Configuration

The watchdog timer is configured from 4-bit binary counter that uses either TBC10, TBC16, TBC18 or TBC20 as the input clock, a flip-flop for controlling the enable / disable of watchdog timer output, and control registers.



Figre 3.5.1 Watchdog Timer Block Diagram

3.5.2 Control Registers

The watchdog timer is controlled by three control registers, named WDTCR1, WDTCR2 and WDTCR3.

Watchdog Timer Control Register 1

WDTCR1 (FFFBH)	7	6	5	4	3	2	1	0	
			TBC1F	TBC0F	WDTE		EXF	DRVE	(Initial Value **00 1*00)

WDTE	Watchdog Timer Enable	0 : Disable 1 : Enable	R/W

Watchdog Timer Control Register 2

WDTCR2 (F797H)	7	6	5	4	3	2	1	0	
					WDTP1	WDTP0	HALTM1	HALTM0	(Initial Value **** 0000)

WDTP1 WDTP0	Watchdog Timer Source Clock Selection	00 : TBC20 (2^{21}/fc or 2^{21}/fs) 01 : TBC18 (2^{19}/fc or 2^{19}/fs) 10 : TBC16 (2^{17}/fc or 2^{17}/fs) 11 : TBC10 (2^{11}/fc or 2^{11}/fs)	R/W

Watchdog Timer Control Register 3

WDTCR3 (FFFCH)	7	6	5	4	3	2	1	0	
									(Initial Value **** ****)

WDTCR3	Watchdog Timer Controlling Code	4EH : Clear binary counter (Clear code) B1H : Disable watchdog (Disable code) Others : No meaning	write only

3.5.3 Operation

The watchdog timer is a kind of timer which generaters an interrupt when its counter overflows. The input clock of 4-bit binary counter can be selected by the Watchdog Timer Control Register 2 WDTCR2<WDTP1,WDTP0> and the time to be detected can be selected.

By a program, the 4-bit counter should be reset before the counter becomes overflow in order to get a watchdog timer function. If the CPU can not execute writing clear code because of the noise, etc., the WDT generates an interrupt and the CPU can be recovered to a normal state by an interrupt routine of watchdog timer.

The watchdog timer starts soon after the reset.

The watchdog timer stops during STOP mode, and when the STOP mode is released it restarts after the warming-up time is over. In other mode, the watchdog timer operates, however it can be disabled by register setting.

(1) Watchdog timer enable / disable Control

By the reset operation, the enable/disable bit <WDTE> in the watchdog timer control register 1 (WDTCR1) is set to "1", and therefore the watchdog timer is enabled.

To disable the watchdog timer, this <WDTE> should be cleared to "0" and the disable code (B1H) should be written into the watchdog timer control register 3 (WDTCR3). To enable the watchdog timer from disable condition, the <WDTE> only need to be set to "1".

(2) Watchdog timer source clock select

The interval time of the watchdog timer can be selected by the clock selection bits <WDTP1>, <WDTP0> in the watchdog timer control register 2 (WDTCR2). In the reset operation, <WDTP1> and <WDTP0> are reset to "00". The following table shows the combination of the source clock and the watchdog timer's interval time.

The interrupt vector address of INTWDT is 000CH.

Table 3.5.1 Interval time of Watchdoge Timer

<WDTP1, 0>	Source Clock	Interval Time of INTWDT	
		at fc = 16 MHz	at fc = 32 kHz
00	TBC 20	2097.15 ms	1048.58 s
01	TBC 18	524.29 ms	262.14 s
10	TBC 16	131.07 ms	65.54 s
11	TBC 10	2.05 ms	1.02 s

3.6 TIMER COUNTER

3.6.1 Timer Counter 0 (TC0) / Timer / Counter 1 (TC1)

The timer counter 0 and timer counter 1 are configured from an 8-bit increment counter, 8-bit timer register and 8-bit compactor circuits. These two timer counters can be operated independently or they can be cascade-connected and used as a 16-bit timer counter.

(1) Block diagram

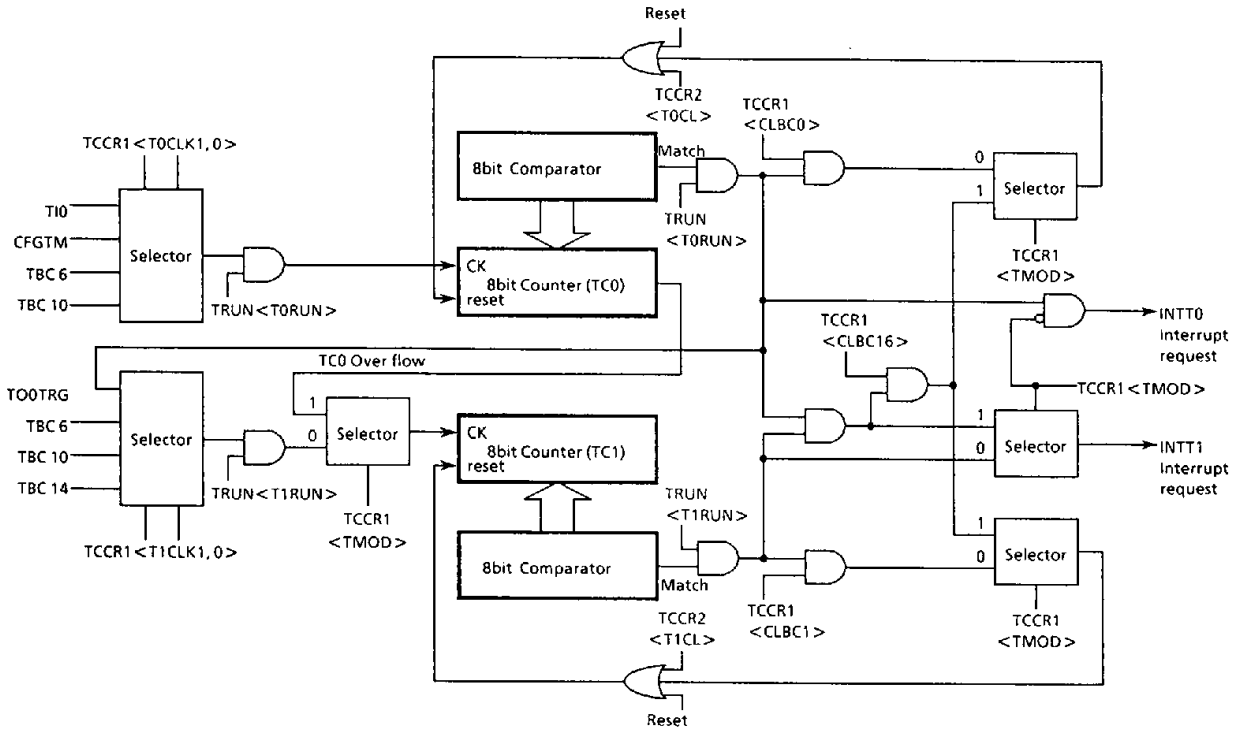


Figure 3.6.1 Configuration of the Timer Counter (TC1 and TC0)

① Up-counter

Each of the TC1 and TC0 has an 8-bit up-counter which input is selected by the timer / counter control register 1 TCCR1<T0CLK1, 0> and <T1CLK1, 0>.

The clock source of the TC0 can be selected from internal clock TBC6 (27/fc), TBC10 (211/fc) TC1, external clock input TI0 and CFGTM from a capture input control circuit (CAPIN). The clock source of the TC1 can be selected from internal clock TBC6 (27/fc), TBC10 (211/fc), TBC14 (215/fc) and TO0TRG (TC0 comparator output). The TC0 and TC1 can be used as 2 8-bit timers or 16-bit timer by setting the TCCR1<TMOD>. As this bit is cleared by RESET, the 8-bit timer mode is selected, initially. When the 16-bit timer mode is selected, the clock source of TC1 is fixed to the overflow output from TC0.

The count-up operation, start/stop, can be controlled independently by the timer start control register TRUN. These up-counters are cleared and stopped by reset operation.

These up-counters can be cleared by the match signals from comparators. The selection of clearing up-counters is set by TCCR1<CLBC1, 0> in 8-bit timer mode or by TCCR1<CLBC16> in 16-bit timer mode. By setting "1" to TCCR2<T0CL> and <T1CL>, these up-counters can be cleared by software.

② Timer Register (TREG0 and TREG1)

The timer register is an 8-bit register and is used to set the interval time for timer. The comparator outputs a match signal when the value in this register and the value of up-counter becomes equal. In case that the setting value in TREG is 00H, the match signal is generated when the up-counter is over-flowed. The data in this register is loaded to the comparator immediately after new data is written into this register.

By reading the TREG, the value of 8-bit counter can be read out. The interval time set in this register can't be read out. The TREG isn't initialized by reset, in other word, the initial value of TREG is unknown.

③ Comparator

The comparator compares the values in up-counter and timer register. When the data becomes equal, and the interrupt request (INTT0, INTT1) is generated.

(Note) The timer interrupt 0 (INTT0) has a same vector address as an interrupt for direction of capstan motor (INTDIR). The selection of INTT0 or INTDIR can be done by setting the interrupt control register INTCR<T0DIR>.

Timer Counter 0 Data Register

TREG0 (FFCAH)	7	6	5	4	3	2	1	0	(Initial Value 0/*0/*0/*0/* 0/*0/*0/*0/*)	Read / Write
	TC/TR07	TC/TR06	TC/TR05	TC/TR04	TC/TR03	TC/TR02	TC/TR01	TC/TR00		

Timer Counter 1 Data Register

TREG1 (FFCBH)	7	6	5	4	3	2	1	0	(Initial Value 0/*0/*0/*0/* 0/*0/*0/*0/*)	Read / Write
	TC/TR17	TC/TR16	TC/TR15	TC/TR14	TC/TR13	TC/TR12	TC/TR11	TC/TR10		

Timer Counter Control Register 1

TCCR1 (FFCCH)	7	6	5	4	3	2	1	0	(Initial Value 0000 0000)
	CLBC16	CLBC1	CLBC0	TMOD	T1CLK1	T1CLK0	T0CLK1	T0CLK0	

CLBC16	16-bit Timer / Counter Clear by match	0 : Disable 1 : Enable	R/W
CLBC1	TC1 Counter Clear by match	0 : Disable 1 : Enable	
CLBC0	TC0 Counter Clear by match	0 : Disable 1 : Enable	
TMOD	Timer Mode Selection	0 : 8-bit Timer Mode 1 : 16-bit Timer Mode	
T1CLK1 T1CLK0	TC1 Source Clock Selection	00 : T00TRG (TC0 Comparator output) 01 : TBC6 10 : TBC10 11 : TBC14	
T0CLK1 T0CLK0	TC0 Source Clock Selection	00 : TI0 (P34 input) 01 : CFGTM (Input from CAPIN) 10 : TBC6 11 : TBC10	

Timer Counter Control Register 2

TCCR2 (FFD1H)

7	6	5	4	3	2	1	0
		T1CL	T0CL	CLBC2	T2CL	T2CLK1	T2CLK0

(Initial Value **00 0000)

T1CL	TC1 Counter Clear	0 : – 1 : Clear (One-shot)	R/W
T0CL	TC0 Counter Clear	0 : – 1 : Clear (One-shot)	

Timer Start Control Register

TRUN (FFD4H)

7	6	5	4	3	2	1	0
PWM3 RUN	T3RUN	PWM1 RUN	PWM0 RUN	PWM2 RUN	T2RUN	T1RUN	T0RUN

(Initial Value 0000 0000)

T1RUN	TC1 Count Start	0 : Stop 1 : Start	R/W
T0RUN	TC0 Count Start	0 : Stop 1 : Start	

(3) Operation

① 8-bit Timer Mode

a. Generating interrupts at specified intervals

Periodic interrupts (INTT0, INTT1) can be generated by using Timer Counter (TC0, TC1) in the following procedure, Stop timer (TC0, TC1), Set the desired operating mode, source clock and interval time in the TCCR1 and TREG0 (TREG1), Enable the interrupt, Start the counting of the timer.

Example : To generate TC1 interrupt (INTT1) every 40 μs at fc = 16 MHz, the registers should be set as follows ;

MSB LSB

TRUN ← – – – – – – 0 – : Stop and clear TC1
TCCR1 ← – 1 – 0 0 1 – – : 8-bit timer mode, TBC6 (8 μs at fc = 16 MHz)
TREG1 ← 0 0 0 0 0 1 0 1 : Set 40 μs / TBC6 = 05H to Timer register
INTE2 ← – – – – – 1 – – : Enable INTT1 interrupt
TRUN ← – – – – – – 1 – : TC1 count start

Note : –; no change

Table 3.6.1 Interrupt Interval (INTT0, INTT1) and Clock Source

Timer Interrupt Interval (at fc = 16 MHz)			Resolution	Clock Input
8 μs	to	2.048 ms	8 μs	TBC6 (2^7 / fc)
128 μs	to	32.768 ms	128 μs	TBC10 (2^{11} / fc)
2.048 ms	to	524.288 ms	2.048 ms	TBC14 (2^{15} / fc)

b. Counting up the TC1 by match signal from TC0

Set the TC1 to 8-bit timer mode and select TC0 comparator output (TO0TRG) as the TC1 clock source. Then, write the timing data in TREG0 first and write data in TREG1.

c. Using TC0 as an event counter

The counter in TC0 counts an input signal from TI0 (P34) terminal at its rising edge. The INTT0 interrupt is generated when the counter value matches the value in TREG0.

The maximum applied frequency is fc/2^4[Hz] (1MHz at fc = 16 MHz) and minimum applied pulse width is 2^3/fc [s] (500 ns at fc = 16 MHz) both "H" and "L" levels.

d. Using TC0 as a counter for Capstan FG signal

The Capstan FG signal which is amplified by CFG amplifier is inputted, as CFGA signal, to the Capture input control circuit (CAPIN).

The CFGA signal is divided by 2 or by passed by Capture input control circuit and inputted to Timer Counter 1 (CFGTM signal).

② 16-bit Timer Mode

TC0 and TC1 can be cascade-connected and used as a 16-bit timer counter. By setting TCCR1<TMOD> to "1", these timers are connected in cascade. In this mode, even if clock source is set for TC1, the clock source of TC1 becomes TC0 overflow output.

Table 3.6.2 INTT1 Interrupt Interval and Clock Source for 16-bit timer counter

Interrupt Interval (at fc = 16 MHz)			Resolution	TC0 input clock
8 μs	to	524.29 ms	8 μs	TBC6 (2^7 / fc)
128 μs	to	8.39 s	128 μs	TBC10 (2^{11} / fc)
2.048 ms	to	134.22 s	2.048 ms	TBC14 (2^{15} / fc)

To set the interval time to timer registers, lower 8-bit should be set to TREG0 and higher 8-bit should be set to TREG1 in this order.

For example, to generate INTT1 interrupt request every 0.5 s, set as following data to TREG0 and TREG1.

TBC6 as clock source (8 μs at 16 MHz)

0.5 s / 8 μs = 62500 = F424H

TREG0 = 24H, TREG1 = F4H

In this case, the output from comparator of TC0 comes active every time when up-counter and TREG0 becomes equal, but the INTT0 isn't generated, and the up-counter isn't cleared in spite of the setting in <CLBC0>.

The output from comparator of TC1 comes active every time when up-counter and TREG1 becomes equal. At the timing that both comparator of TC0 and TC1 becomes active, up-counters are cleared and INTT1 is generated.

3.6.2 Timer Counter 2 (TC2)

The timer counter 2 (TC2) is configured from an 8-bit up-counter, timer register and comparator circuits.

(1) Configuration

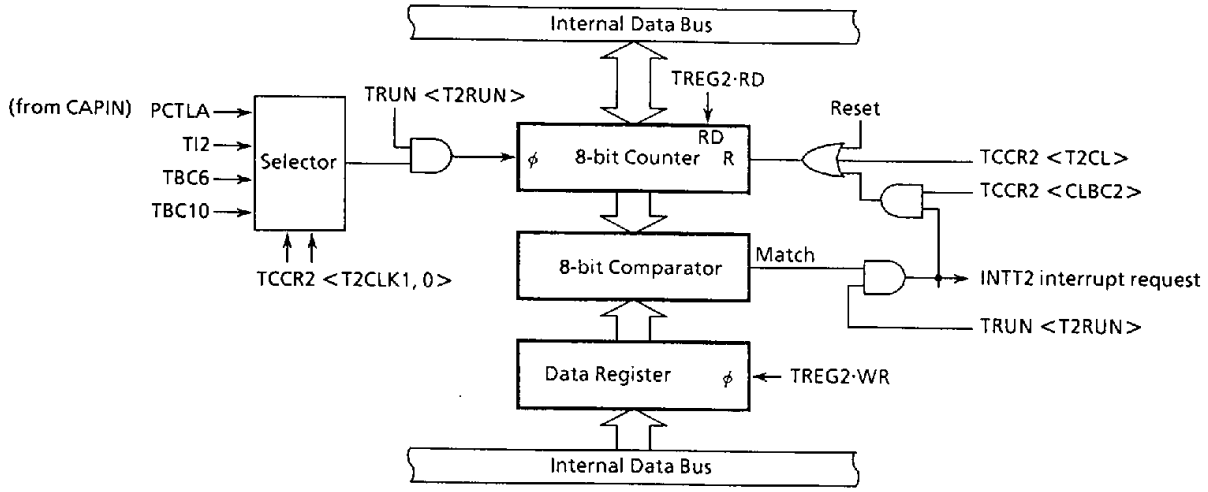


Figure 3.6.2 Configuration of the Timer Counter 2 (TC2)

① 8-bit up-counter

The 8-bit up-counter counts clock selected by the timer counter control register 2 TCCR2<T2CLK1, 0>. The clock can be selected from the TBC6 (27/fc), TBC10 (211/fc), TI2 (P35 input) and PCTLA from Capture input control circuit (CAPIN).

The counter can be started / stopped by the Timer start control register (TRUN). The counter is cleared and stopped by reset operation.

By writing "1" to TCCR2<T2CL>, this counter can be cleared. Clearing the 8-bit counter by match signal from comparator is enabling by TCCR2<CLBC2>.

② Data Register (TREG2)

The data register TREG2 is a 8-bit register used for setting the interval time. When the up-counter becomes same value with TREG2, the comparator outputs match signal. The data written to this register is transferred immediately to the comparator. In case that the TREG2 is set as "00H", the comparator output becomes active when up-counter is overflowed. Value of the 8-bit up-counter can be read by reading TREG2. The TREG2 isn't initialized by reset, in other word, the initial value of TREG2 is unknown.

③ Comparator

The comparator compares the value of up-counter with the value of TREG2, and generates the interrupt (INTT2). Clearing the up-counter by the match signal is controlled by TCCR2<CLBC2>.

(2) Control register

Timer Counter 2 Data Register

TREG2 (FFCDH)

7	6	5	4	3	2	1	0
TC/TR27	TC/TR26	TC/TR25	TC/TR24	TC/TR23	TC/TR22	TC/TR21	TC/TR20

(Initial Value 0/*0/*0/*0/* 0/*0/*0/*0/*) Read/Write

Timer Counter Control Register 2

TCCR2 (FFCCH)

7	6	5	4	3	2	1	0
		T1CL	T0CL	CLBC2	T2CL	T2CLK1	T2CLK0

(Initial Value **00 0000)

CLBC2	TC2 Counter Clear by match signal	0 : Disable 1 : Enable	R/W
T2CL	TC2 Counter Clear	0 : – 1 : Clear (One-shot)	
T2CLK1	TC2 Source Clock Selection	00 : PCTLA (from CAPIN) 01 : TI2 (P35 input) 10 : TBC6 11 : TBC10	
T2CLK0			

Timer Start Control Register

TRUN (FFD4H)

7	6	5	4	3	2	1	0
PWM3 RUN	T3RUN	PWM1 RUN	PWM0 RUN	PWM2 RUN	T2RUN	T1RUN	T0RUN

(Initial Value 0000 0000)

T2RUN	TC2 count start	0 : Stop 1 : Start	R/W

(3) Operation

① Generating interrupt at specified intervals

Periodic interrupt can be generated in the following procedure : Stop Timer Counter 2, set the input clock and interval to the TCCR2 and TREG2, enables the INTT2 interrupt, and start the counting of Timer Counter 2.

Example : To generate TC2 interrupt every 40 μs at fc = 16 MHz, the registers should be set as follows.

		MSB LSB	
TRUN	←	– – – – – 0 – – :	Stop and clear TC2
TCCR2	←	– – – – 1 * 1 0 :	TBC6 (8 μs at 16 MHz)
TREG2	←	0 0 0 0 0 1 0 1 :	Set TREG2 ("05H" = 40 μs / TBC6)
INTE2	←	– – – – 1 – – – :	Enable INTT2
TRUN	←	– – – – – 1 – – :	Start TC2

Comment : *: Don't care, -: no change

Table 3.6.2 Interrupt Interval (INTT2) and Clock Source

Timer Interrupt Interval (at fc = 16 MHz)			Resolution	Clock Input
8 μs	to	2.048 ms	8 μs	TBC6 (2^7 / fc)
128 μs	to	32.768 ms	128 μs	TBC10 (2^{11} / fc)

② Using TC2 as an event counter

The up-counter counts an input signal from TI2 (P35) at its rising edge. The INTT2 interrupt is generated when the counter matches the value in TREG2.

The maximum applied frequency is fc/24 [Hz] (1 MHz at fc = 16 MHz) and minimum applied pulse width for both "H" and "L" levels is 23/fc [s] (500 ns at fc = 16 MHz).

③ Using TC2 as a counter for CTL signal

The CTL signal amplified by CTL Amplifier, is inputted to the Capture input control circuit (CAPIN) as a CTLOUT signal. A source clock (PCTLA signal) can be selected from CTLIN (P30) input or CTLOUT signal at the CAPIN.

3.6.3 Timer Counter 3 (TC3)

The timer counter 3 (TC3) consists of the an 8-bit up-counter, 8-bit data register (TREG3), 8-bit comparator and timer flip-flop (TFF).

The TC3 can also perform as 8-bit pulse width modulation (PWM) output.

(1) Circuit Blocks

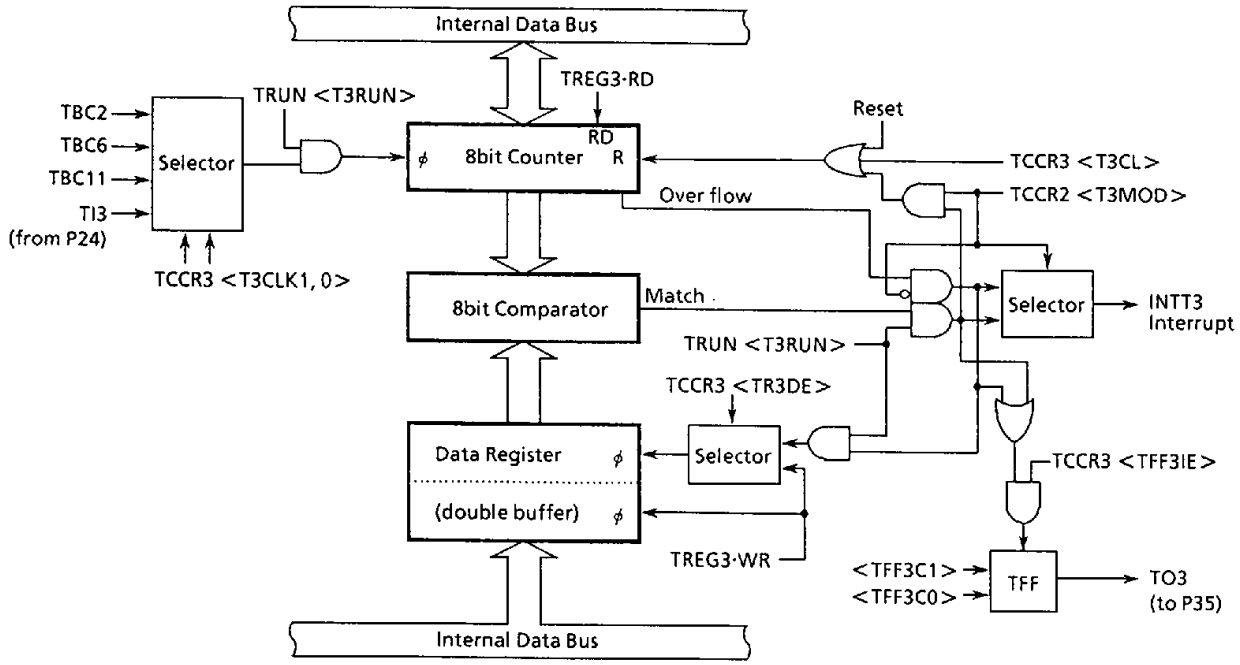


Figure 3.6.3 Configuration of the Timer Counter 3

① 8-bit up-counter

It is an 8-bit up-counter with the clock source selected by TCCR3<T3CLK1, 0>. The clock source can be selected from the timer base counter output TBC2 (23/fc), TBC6 (27/fc), TBC11 (212/fc) and the external input TI3 (P24 pin).

This counter can be started / stopped by setting the timer start control register (TRUN) and is cleared and stopped by reset operation. In case that timer mode is selected by TCCR3<T3MOD>, up-counter is cleared by match signal from comparator. But in PWM mode, counter is not cleared by match signal.

By writing "1" to TCCR3<T3CL>, this counter can be cleared.

② Data Register (TREG3)

Data register is composed of double buffer. And trigger of sifting data is selected by setting the TCCR3<TR3DE>. Set <TR3DE> to "0" in timer mode and to "1" in PWM mode.

In timer mode, a match signal is outputted from comparator when up-counter matches with value of TREG3. The value is transferred to the comparator immediately after writing data to TREG3.

In PWM mode, the data in TREG3 is transferred to comparator every over flow timing of up-counter. A match signal is outputted from comparator when up-counter matches with value of TREG3.

In addition, reading the data register (TREG3) can be in real-time the value of the 8 bit counter. (The specified value of data register can not be read out). The data register isn't cleared by reset operation.

③ Comparator

8-bit comparator compares up-counter and TREG3. In timer mode, when match is occurred, comparator clears up-counter and generates interrupt request (INTT3).

In PWM mode, TO3 output is inverted when match is occurred. The INTT3 interrupt is generated when up-counter overflows.

④ Timer Flip-flop (TFF)

This flip-flop is flipped by the match signal from comparator and the overflow signal from up-counter, when<TFF3IE> = "1". When <TFF3IE> = "0", the flip-flop is disabled. The output of flip-flop can be outputted to TO3 (P35). This TFF output is controlled by TCCR3<TFF3IE>.

Note : The TC3 interrupt (INTT3) has the same vector address as A/D conversion interrupt (INTAD). INTT3 and INTAD need to be chosen by interrupt control register (INTCR) <T3ADS>.

(2) Control Registers

Timer Counter 3 Data Register

TREG3 (FFD2H)

7	6	5	4	3	2	1	0
TC/TR37	TC/TR36	TC/TR35	TC/TR34	TC/TR33	TC/TR32	TC/TR31	TC/TR30

(Initial Value 0/*0/*0/*0/* 0/*0/*0/*0/*) Read/Write

Timer Counter Control Register 3

TCCR3 (FFD3H)

7	6	5	4	3	2	1	0
TR3DE	TFF3C1	TFF3C0	TFF3IE	T3MOD	T3CL	T3CLK1	T3CLK0

(Initial Value 0**0 0000)

TR3DE	TREG3 sifting Trigger Selection	0 : Writing data to TREG3 1 : Overflow of up-counter	R/W
TFF3C1 TFF3C0	TC3 Flip-flop (TFF) Control	00 : Invert the output (TO3) 01 : Set to "1" 10 : Reset to "0" 11 : Keep TO3 output	write only
TFF3IE	Timer Filp-Flop Invert Enable	0 : Disable 1 : Enable	R/W
T3MOD	TC3 Mode Selection	0 : PWM mode 1 : Timer mode	
T3CL	TC3 Counter Clear	0 : – 1 : Clear (One-shot)	
T3CLK1 T3CLK0	TC3 Clock Source Selection	00 : TBC2 01 : TBC6 10 : TBC11 11 : TI3 (Input P24 pin)	

Timer Start Control Register

TRUN (FFD4H)

7	6	5	4	3	2	1	0
PWM3 RUN	T3RUN	PWM1 RUN	PWM0 RUN	PWM2 RUN	T2RUN	T1RUN	T0RUN

(Initial Value 00** 0000)

T3RUN	TC3 count Start	0 : Stop 1 : Start	R/W

(3) Operation

① Timer Mode

The TC3 functions as 8 bit-timer / counter by setting TCCR3 <T3MOD> to "1".

a. Generating interrupt at specified intervals

By setting interval time to TREG3, INTT3 interrupt request is generated when the data in comparator are matched with value of up-counter. By setting TCCR3<TFF3IE> to "1", TFF can be inverted (TO3 output can be inverted) with every matching.

For example, to generate INTT3 interrupt every 256 μs, set registers as follows,

	MSB LSB	
TRUN ←	– 0 – – – – – – :	Stop and clear TC3
TCCR3 ←	0 1 1 0 1 0 0 1 :	Set timer mode and TBC 6 (8us at 16 MHz)
TREG3 ←	0 0 0 0 0 1 0 1 :	Set TREG3 to "20H" = 256 μs / TBC6
INTCR ←	– – – – – – 0 – :	} Enable INTT3 interrupt
INTE2 ←	– – – 1 – – – – :	
TRUN ←	– 1 – – – – – – :	Start TC3

Note : –; no change

Table 3.6.4 INTT3 Interrupt Interval and Source Clock

Interrupt Interval (at fc = 16 MHz)	Resolution	Clock Input
0.5 μs ~ 128 μs	0.5 μs	TBC2 (2^3/fc)
8 μs ~ 2.048 ms	8 μs	TBC6 (2^7 / fc)
256 μs ~ 65.536 ms	256 μs	TBC11 (2^{12} / fc)

b. Using TC3 as an event counter

It counts rising edge of the TI3 (P24) input. A data match between TREG3 and up-counter generates an INTT3 interrupt request. The maximum applied frequency is fc/24 [Hz] (1 MHz at fc = 16 MHz), and the minimum applied pulse width for both "H" and "L" level is 2^3/fc [s] (500 ns at fc = 16 MHz).

② 8-bit Pulse Width Modulation (PWM) mode

TC3 can be used as 8-bit PWM and the wave-form can be outputted through TO3 (P35). The output flips when up-counter matches TREG3 and it's overflow. When TC3 is used as PWM output, setting TC3CR<TFF3IE> and <TR3DE> to "1". Following is a timing chart for PWM mode.

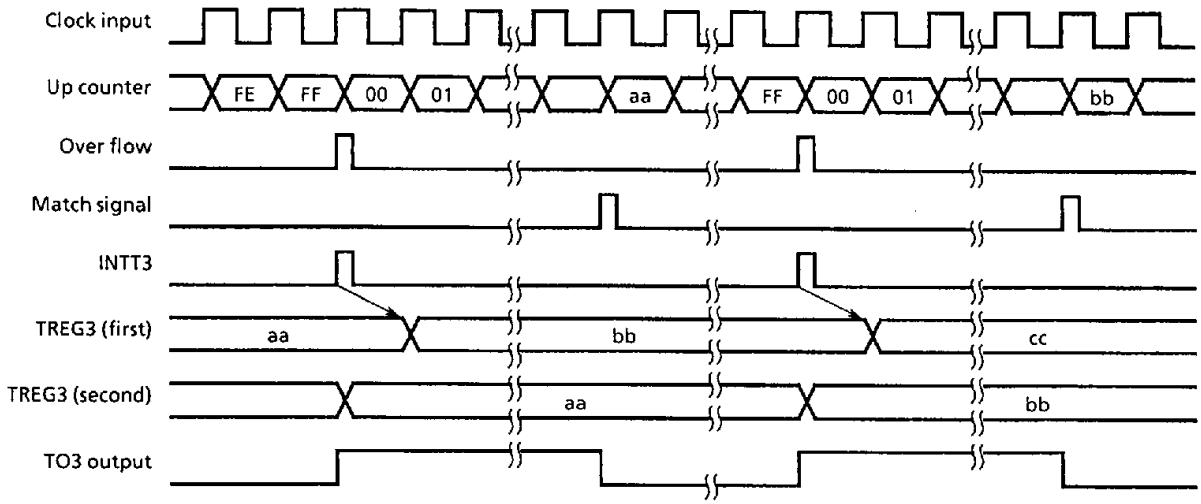


Figure 3.6.4 Timer counter 3 Waveform of 8-bit PWM Output

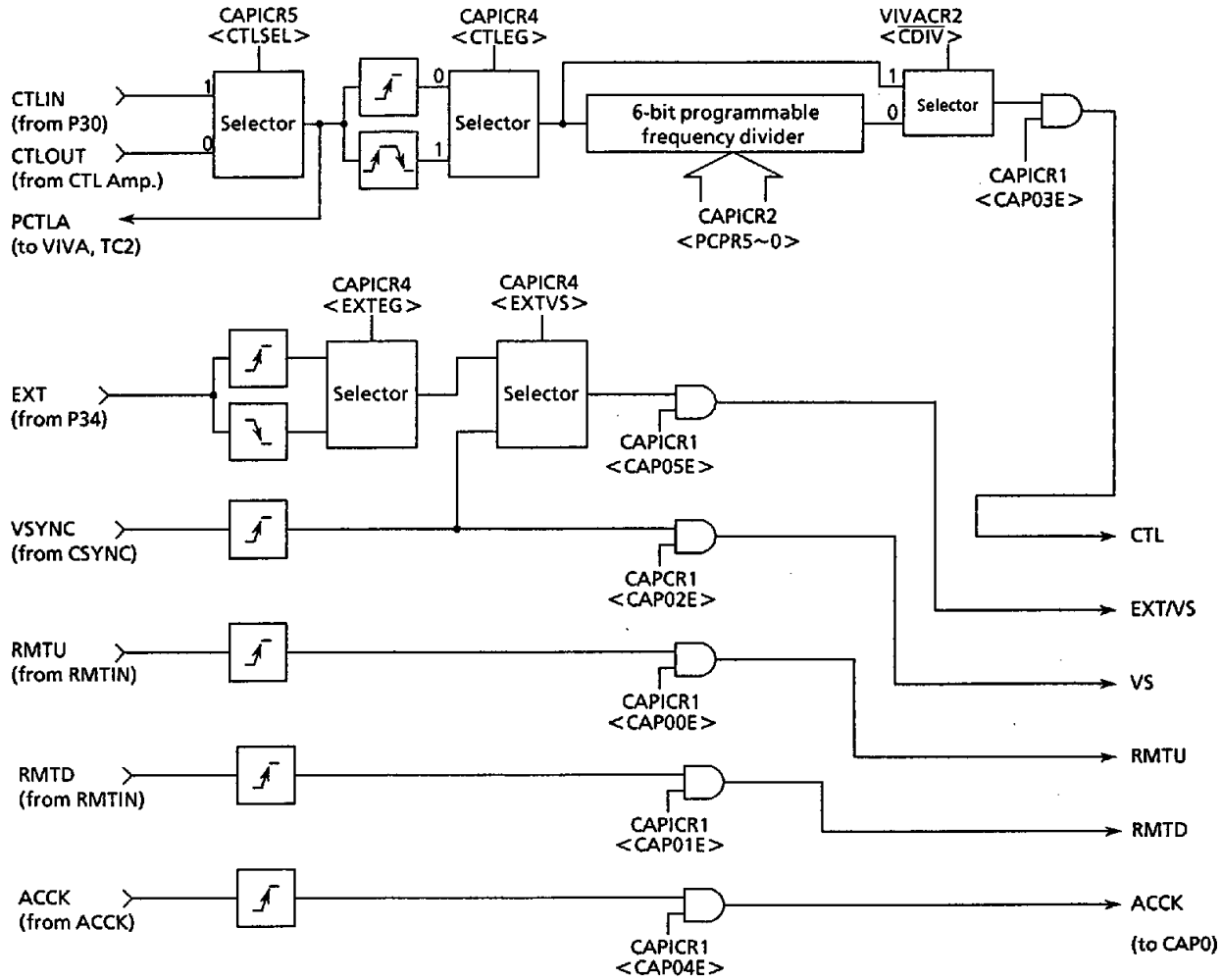
3.7 CAPTURE CIRCUIT

The capture circuit latches the time data of the time base counter (TBC) and the captures input status (Trigger input signal). The data of TBC can be latched by the trigger input signal and the interrupt request is generated to CPU. By using the capture circuit, the time can be measured in high resolution for servo control.

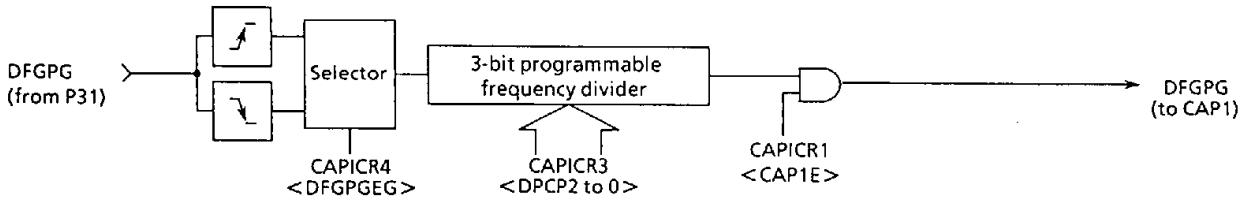
The capture circuit consists of the capture 0 (CAP0) with eight (8) level of 24-bit FIFO (first-in first-out) as buffer, the capture 1 (CAP1) and the capture 2 (CAP2) with single level of 17-bit FIFO as buffers.

3.7.1 Capture Input Control Circuit (CAPIN)

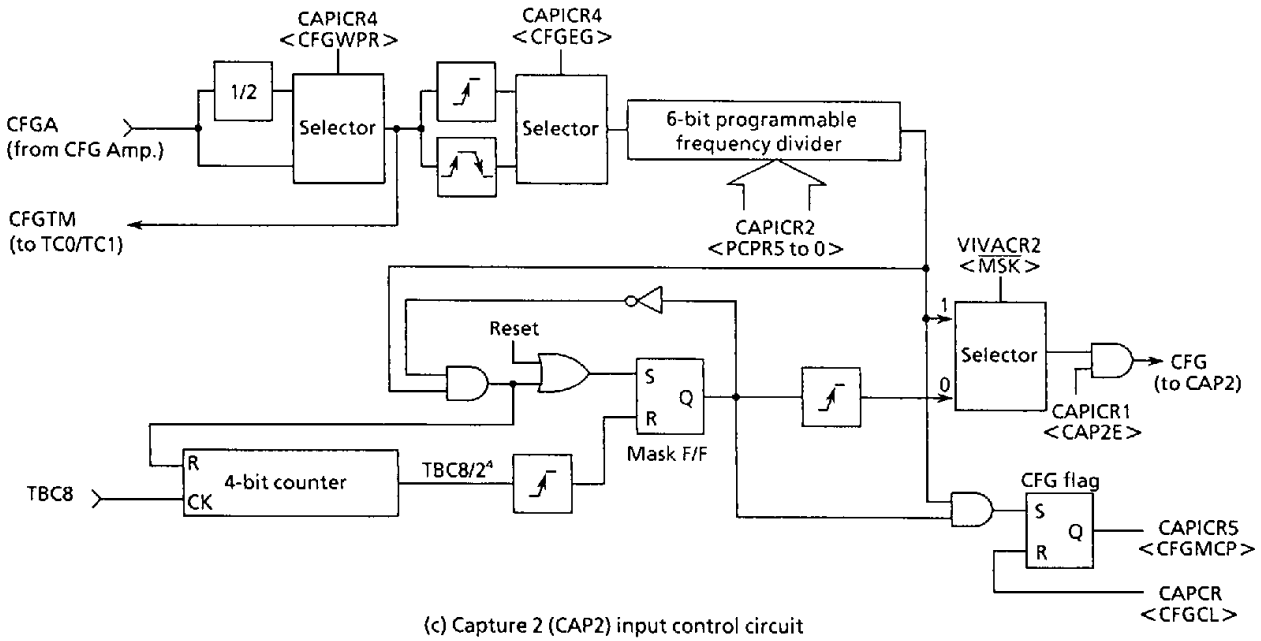
Capture input control circuit (CAPIN) controls the trigger input signals of the three channels of capture circuits (CAP0, CAP1 and CAP2), and comprises the capture 0 input control circuit, capture 1 input control circuit and capture 2 input control circuit.



(a) Capture 0 (CAP0) input control circuit



(b) Capture 1 (CAP1) input control circuit



(c) Capture 2 (CAP2) input control circuit

Figure 3.7.1 Capture input control circuit

(1) Capture 0 (CAP0) Input Control

① Remote control signal leading edge (RMTU)

This is the leading edge signal of the remote control signal detected by the remote control signal input circuit (RMTIN).

Enabling this trigger input to capture 0 (CAP0) is controlled by Capture input control register 1 CAPICR1<CAP00E>.

② Remote control signal trailing edge (RMTD)

This is the trailing edge signal of the remote control signal detected by the remote control signal input circuit (RMTIN).

Enabling this trigger input to capture 0 (CAP0) is controlled by Capture input control register 1 CAPICR1<CAP01E>.

③ Sync. separation input (VS)

This is the vertical Synchronizing signal (VSYNC) separated from Composite Sync signal by Sync signal sparator (CSYNC).

Enabling this trigger input to capture 0 (CAP0) controlled by CAPICR1<CAP02E>.

④ Control signal (CTL)

This is the control signal (CTLOUT) that has been amplified at the CTL amplifier or an external signal from P30 (CTLIN). External input (CTLIN) can be selected by the capture input control register 5 (CAPICR5) <CTLSEL>. The capturing timing can be selected from either leading edge of control signal or both leading and trailing edges by the capture input control register 4 (CAPICR4) <CTLEG>. The detected edge signal can be divided by a 6-bit programmable frequency divider. The frequency division ratio can be set by the capture input control register 2 (CAPICR2) <PCPR5-0>. The frequency division ratios can be set from <PCPR5-0> = 00H (1/1 frequency division) to <PCPR5-0> = 3FH (1/64 frequency division). Selection of whether edge signal is divided or bypassed is carried out by the VISS/VASS control register 2 (VIVACR2) <$\overline{\text{CDIV}}$>.

Enabling the trigger input to capture 0 (CAP0) is controlled by CAPICR1 <CAP03E>.

⑤ AC Clock Input (ACCK)

This is the AC signal from which noise has been removed by the AC clock input circuit (ACCK).

Enabling the trigger input to capture 0 (CAP0) is controlled by CAPICR1 <CAP04E>.

⑥ External Input/V-sync Input (EXT/VS)

The EXT/VS doubles as the external input (EXT) and V-sync signal (VS). Either of these can be selected by CAPICR4 <EXTVS>.

Enabling the trigger input to capture 0 (CAP0) is controlled by CAPICR1 <CAP05E>.

a. External input (EXT)

This is the external trigger input that is inputted from the P34 (TI0/EXT) terminal. The input polarity of the trigger can be switched by CAPICR4 <EXTEG>.

b. V-sync signal (VS)

This is the vertical synchronizing signal (VSYNC) that has been separated from the composite synchronizing signal by the Sync signal separator (CSYNC).

(2) Capture 1 (CAP 1) Input Control

The trigger of capture 1 (CAP1) is a cylinder speed and phase signal (DFGPG). Detection of the leading edge or trailing edge of the DFGPG signal from terminal P31 (DFGPG) is carried out by CAPICR4 <DFGPGEG>. The detected edge signal can be divided by a 3-bit programmable frequency divider. The frequency division ratio can be set by <DPCP2-0> of capture input control register 3 (CAPICR3). The frequency division ratios can be set from <DPCP2-0> = 0H (1/1 frequency division) to <DPCP2-0> = 7H (1/8 frequency division). Enabling the trigger input to capture 1 (CAP1) is controlled by <CAP1E> of capture input control register (CAPICR1).

(3) Capture 2 (CAP2) Input Control

The trigger of capture 2 (CAP2) is the capstan frequency signal (CFGA) amplified by the CFG amplifier. The input signal can be divided 1/1 or 1/2 by using <CFGWPR> of capture input control register 4 (CAPICR4). Either the leading edge or both the leading and trailing edges of the CFGA signal can be selected by CAPICR4<CFGEG>. The detected signal can be divided by a 6-bit programmable frequency divider. The frequency division ratio can be set by <PCPR5-0> of CAPICR2 in common with the capturing for CTL. The divided CFGA signal can be masked during an interval of TBC8 (2^9/fc) x 8 [s] by a 4-bit mask counter. CFGA signals during the mask interval are not inputted to CAP2, but CFG flag (CAPICR5 <CFGMCP>) is set to "1". The CFG flag can be reset to "0" by <CFGCL> of capture control register 1 (CAPCR). The selection between subjecting the CFGA signal to mask processing or by passing it can be selected by <MSK> of VISS/VASS control register 2 (VIVACR2).

Enabling the trigger input to capture 2 (CAP2) is controlled by <CAP2E> of capture input control register 1 (CAPICR1).

Fig. 3.7.2 shows the timing chart for capture 2 input control.

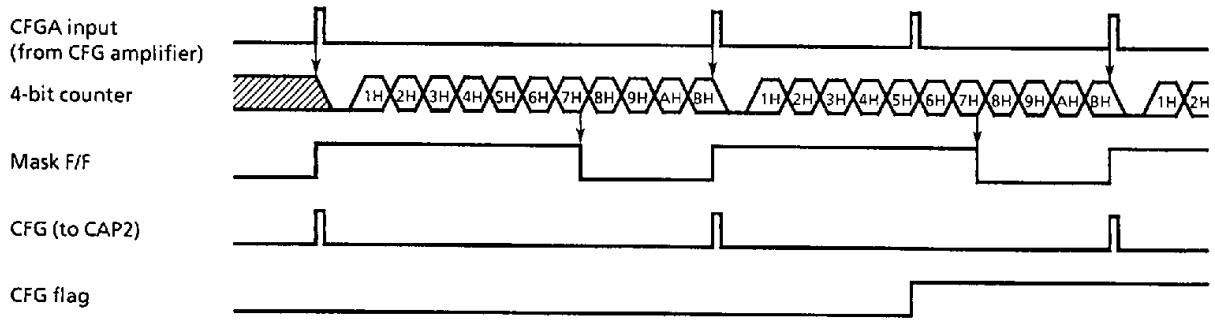


Figure 3.7.2 Capture 2 Input Control Timing Chart (<$\overline{\text{MSK}}$> = 0)

(4) Capture Input Control Register

Capture input control register 1

CAPICR1 (FFBFH)

7	6	5	4	3	2	1	0
CAP2E	CAP1E	CAP05E	CAP04E	CAP03E	CAP02E	CAP01E	CAP00E

(Initial value 0000 0000)

CAP2E	Enable/disable the capture 2 (CAP2) trigger input	0 : Disable 1 : Enable	R/W
CAP1E	Enable/disable the capture 1 (CAP1) trigger input	0 : Disable 1 : Enable	
CAP05E to CAP00E	Enable/disable the capture 0 (CAP0) trigger input	0 : Disable 1 : Enable	

Capture input control register 2

CAPICR2 (FFF6H)

7	6	5	4	3	2	1	0
PCTL CK1	PCTL CK0	PCPR5	PCPR4	PCPR3	PCPR2	PCPR1	PCPR0

(Initial value 0000 0000)

PCPR5 to PCPR0	Control of 6-bit programmable frequency divider	Setting the frequency division ratio (from 1/1 to 1/64) for CTLIN (from P30) / CLTOUT (from CTL amp.) and CFGA (from CFG amp.)	R/W

Capture input control register 3

CAPICR3 (FFF7H)

7	6	5	4	3	2	1	0
					DPCP2	DPCP1	DPCP0

(Initial value **** *000)

DPCP2 to DPCP0	Control of 3-bit programmable frequency divider	Setting the frequency division ratio of DFGPG (from P31) from 1/1 to 1/8	R/W

Capture input control register 4

CAPICR4 (FFF9H)

7	6	5	4	3	2	1	0
		EXTVS	EXTEG	DFGP GEG	CFG WPR	CFGEG	CTLEG

(Initial value **00 0000)

EXTVS	EXT/VS (to CAP0) input selection	0 : Input VSYNC (from CSYNC) 1 : Input EXT (from P34)	R/W
EXTEG	Edge selection for EXT input (from P34)	0 : Leading edge 1 : Trailing edge	
DFGPGEG	Edge selection for DFGPG input (from P31)	0 : Leading edge 1 : Trailing edge	
CFGWPR	Frequency division ratio selection for CFGA input (from CFG amplifier)	0 : 1/1 frequency division 1 : 1/2 frequency division	
CFGEG	Edge selection for CFGA input (from CFG amplifier)	0 : Both edges 1 : Leading edge	
CTLEG	Edge selection for CTLIN/CTLOUT input (from P30/CTL amplifier)	0 : Leading edge 1 : Both edges	

Capture input control register 5

CAPICR5 (FFFAH)

7	6	5	4	3	2	1	0
		CTLSEL	RMTST	RMTP0	ACCKBP	RMTBP	CFGMCP

(Initial value **00 0000)

CTLSEL	Selection of CTL input (to CAP0)	0 : CTLOUT (from CTL amplifier) 1 : CTLIN (from P30)	R/W
CFGMCP	CFG flag	0 : Normal operation (no CFGA in mask interval) 1 : Error detected (CFGA input in mask interval)	read only

Capture control register

CAPCR (FFBEH)

7	6	5	4	3	2	1	0
CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS

(Initial value 0000 0000)

CFGCL	Clear CFG flag	0 : – 1 : Clear (one-shot)	R/W

VISS/VASS control register 2

VIVACR2 (FFF5H)

7	6	5	4	3	2	1	0
PCTLPO	PCTL CKS	$\overline{CDIV}$	$\overline{MSK}$	VISS3	VISS2	VISS1	VISS0

(Initial value 0000 0000)

$\overline{CDIV}$	Control of frequency division of CTLIN (from P30) / CTLOUT (from CTL amp.)	0 : Frequency division from 1/1 to 1/64 1 : Bypass	R/W
$\overline{MSK}$	Mask control of CFGA signal (from CFG amplifier)	0 : With noise Mask 1 : Bypass	

3.7.2 Capture 0 (CAP0)

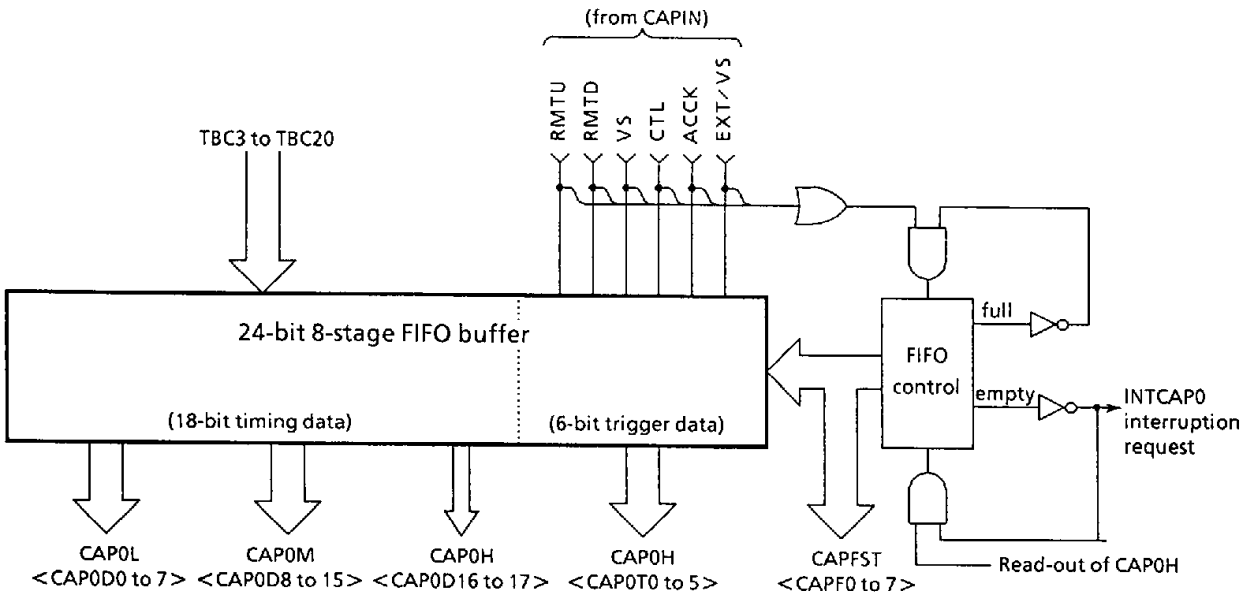


Figure 3.7.3 Structure of Capture 0

(1) Description of Operation

① Capture

The trigger signals for capture 0 are the six signals that are outputted from the capture 0 input control circuit, RMTU, RMTD, VS, CTL, ACCK and EXT/VS signals. The CAP0 latches 18 bits of timing data (Output from Time Base Counter : TBC3 to TBC20) in 3 bytes of Capture Data Register (Memory address FFB7H to FFB9H) and 6 bits of trigger data. It latches a total of 24 bits data.

The 24 bits of latched data can be obtained by reading the data from memory addresses FFB7H, FFB8H and FFB9H in this order.

Note: By reading data from memory address FFB9H the address of the FIFO buffer is shifted, so please ensure that this data is read last.

② FIFO Status Register

The 24-bit 8-stage buffer features a FIFO (First In First Out) function, allowing the data latched first to be read first. The FIFO status register (CAPFST) indicates the shift status of FIFO, and the status bits that correspond to the stage being latched are set to "1". When the 8-stage FIFO buffer become full, capture operations are disabled and the FIFO status register shows "FFH".

When the FIFO status register shows "00H", in other words the 8-stage FIFO buffer is empty, the reading data of the capture data register is "FFH". The capture data can be read out when INTCAP0 interruption has been generated after data has been latched by a trigger signal, or when the FIFO status register is not "00H."

③ Capture Reset

In addition to a system reset function (initialization by resetting), capture 0 also possesses a software reset function. Software reset is performed by writing "1" at <CAFRS> of the capture control register (CAPCR). In performing a software reset, the following circuits are initialized.

a. The FIFO address counter is addressed to the first stage of the 8-stage FIFO buffer.
b. The FIFO status register (CAPFST) is initialized to "00H."

④ INTCAP0 Interruption

When latch operations are carried out by a trigger input signal, an INTCAP0 interruption request is generated. The INTCAP0 interruption request signal is maintained in an active state until the FIFO status register reaches "00H" (empty).

Once INTCAP0 interruption is received, capture data in CAP0L, CAP0M and CAP0H <CAP0D16 to 17> and trigger input data in CAP0H<CAP0T0 to 5> can be read-out and verified the time data and interrupt sources.

INTCAP0 interruption requests are canceled by reading out the FIFO buffer until the content of the FIFO status register reaches "00H" or writing "1" to <CAFRS> of CAPCR.

⑤ Data Processing

The upper 6 bits of the 24 bits of data latched by the FIFO buffer are the status data for the trigger signal. The data of the bit that corresponds to the trigger input signal is set to "1," so by reading out this data the input signal can be identified.

Store the latched data in RAM, and by subtracting the data previously stored in the RAM from the data latched by the next trigger signal, highly precise time measurement can be carried out. Detection precision is 500ns when operating at 16 MHz, and quantum error is extremely small.

(2) Control Register

Capture 0 FIFO status register

CAPFST (FFB6H)

7	6	5	4	3	2	1	0
CAPF7 (8th stage)	CAPF6 (7th stage)	CAPF5 (6th stage)	CAPF4 (5th stage)	CAPF3 (4th stage)	CAPF2 (3rd stage)	CAPF1 (2nd stage)	CAPF0 (1st stage)

(Initial value 0000 0000)

CAPF7 to CAPF0	FIFO status	0 : no capture data 1 : capture data present	read only

Capture 0 data register - low order

CAP0L (FFB7H)

7	6	5	4	3	2	1	0
CAP0D7 (TBC10)	CAP0D6 (TBC9)	CAP0D5 (TBC8)	CAP0D4 (TBC7)	CAP0D3 (TBC6)	CAP0D2 (TBC5)	CAP0D1 (TBC4)	CAP0D0 (TBC3)

(Initial value **** ****) read only

Capture 0 data register - middle order

CAP0M (FFB8H)

7	6	5	4	3	2	1	0
CAP0 D15 (TBC18)	CAP0 D14 (TBC17)	CAP0 D13 (TBC16)	CAP0 D12 (TBC15)	CAP0 D11 (TBC14)	CAP0 D10 (TBC13)	CAP0 D9 (TBC12)	CAP0 D8 (TBC11)

(Initial value **** ****) read only

Capture 0 data register - high order

CAP0H (FFB9H)

7	6	5	4	3	2	1	0
CAP0T5 (EXT/ VS)	CAP0T4 (ACCK)	CAP0T3 (CTL)	CAP0T2 (VS)	CAP0T1 (RMTD)	CAP0T0 (RMTD)	CAP0 D17 (TBC19)	CAP0 D16 (TBC20)

(Initial value **** ****) read only

CAP0T5 to CAP0T0	Trigger input status	0 : no trigger input 1 : trigger input	read only

Capture control register

CAPCR (FFBEH)

7	6	5	4	3	2	1	0
CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS

(Initial value 0000 0000)

CAFRS	FIFO counter/status clear	0 : – 1 : clear (one-shot)	R/W

3.7.3 Capture 1/Capture 2 (CAP1/CAP2)

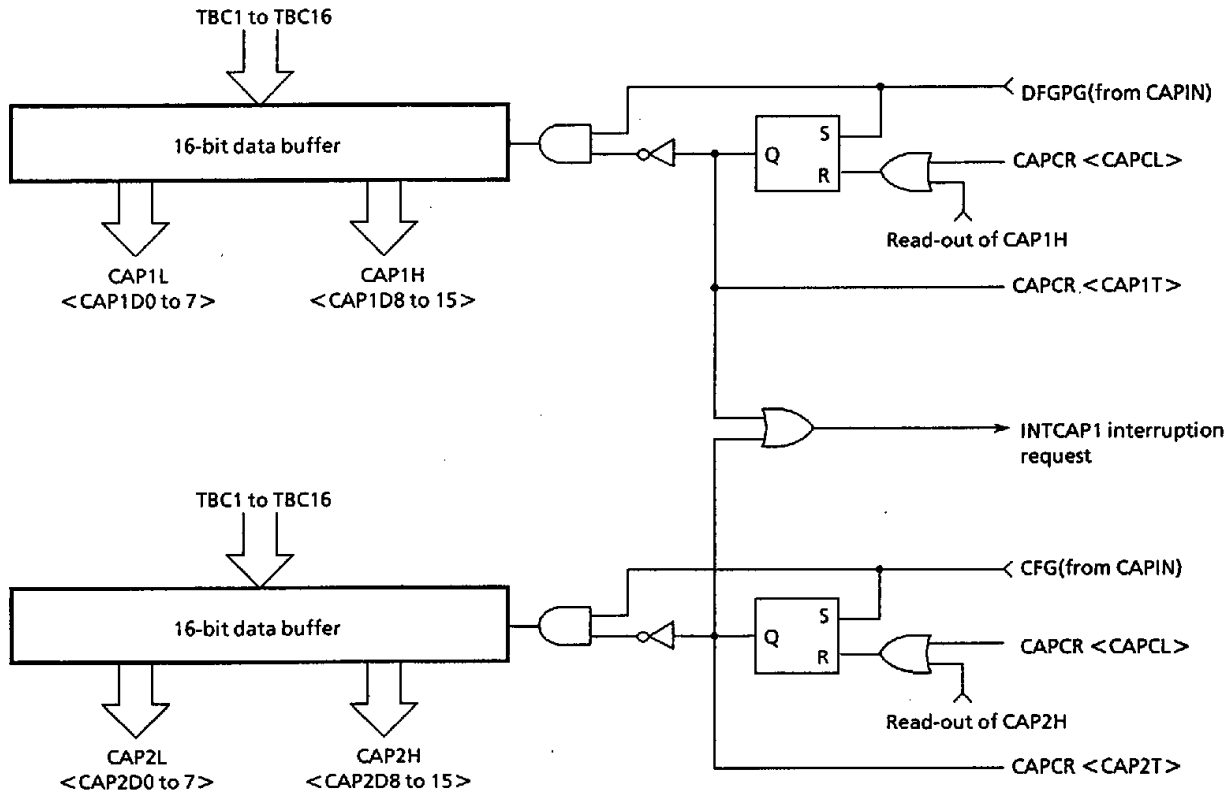


Fig. 3.7.4 Structure of Capture 1/Capture 2

(1) Operation

① Capture

The trigger input signals are DFGPG and CFG signals for capture 1 and capture 2 respectively.

The output values of time base counters (TBC1-TBC16) are latched onto the 2 bytes of capture data register (capture 1 has memory addresses FFBAH and FFBBH, while capture 2 has memory addresses FFBCH and FFBDH) using the edge of the trigger input signal.

The trigger input signal is latched onto <CAP1T> and <CAP2T> of the capture control register (CAPCR).

When the CAPCR<CAP1T> is "1", the Capture 1 data can be obtained by reading out the data from the low order of the capture 1 data register (CAP1L) and from the high order capture 1 data register (CAP1H) in this order. By reading out CAP1H, the trigger input status <CAP1T> is cleared. When <CAP1T> is "0" the read-out of CAP1L and CAP1H is "FFH."

When the CAPCR<CAP2T> is "1", the Capture 2 data can be obtained by reading out the data from the low order of the capture 2 data register (CAP2L) and from the high order capture 2 data register (CAP2H) in this order. By reading out CAP2H, the trigger input status <CAP2T> is cleared. When <CAP2T> is "0" the read-out of CAP2L and CAP2H is "FFH."

② Capture Reset

In capture 1 and 2, trigger input signal <CAP1T> and <CAP2T> can be cleared by writing "1" to <CAPCL> of CAPCR.

③ INTCAP1 Interruption

When latch operations are carried out by the edge of a DFGPG signal or CFG signal, a INTCAP1 interruption request is generated.

INTCAP1 interruption is common to both capture 1 and capture 2, so please read out <CAP1T> and <CAP2T>, and discriminate between them before carrying out processing.

INTCAP1 interruption requests are released by reading out either CAP1H or CAP2H and clearing <CAP1T> <CAP2T> to "0," or by writing <CAPCL> of CAPCR to "1."

(2) Control registers

① Control register of capture 1

Capture 1 data register - low order

CAP1L (FFBAH)

7	6	5	4	3	2	1	0
CAP1D7 (TBC8)	CAP1D6 (TBC7)	CAP1D5 (TBC6)	CAP1D4 (TBC5)	CAP1D3 (TBC4)	CAP1D2 (TBC3)	CAP1D1 (TBC2)	CAP1D0 (TBC1)

(Initial value **** ****) read only

Capture 1 data register - high order

CAP1H (FFBBH)

7	6	5	4	3	2	1	0
CAP1 D15 (TBC16)	CAP1 D14 (TBC15)	CAP1 D13 (TBC14)	CAP1 D12 (TBC13)	CAP1 D11 (TBC12)	CAP1 D10 (TBC11)	CAP1 D9 (TBC10)	CAP1 D8 (TBC9)

(Initial value **** ****) read only

Capture control register

CAPCR (FFBEH)

7	6	5	4	3	2	1	0
CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS

(Initial value 0000 0000)

CAP1T (DFGPG)	CAP1 trigger input status	0 : No trigger input 1 : Trigger input	read only
CAPCL	CAP1/CAP2 status clear	0 : – 1 : Clear (one-shot)	R/W

② Control register of capture 2

Capture 2 data register low order

CAP2L (FFBCH)

7	6	5	4	3	2	1	0
CAP2D7 (TBC8)	CAP2D6 (TBC7)	CAP2D5 (TBC6)	CAP2D4 (TBC5)	CAP2D3 (TBC4)	CAP2D2 (TBC3)	CAP2D1 (TBC2)	CAP2D0 (TBC1)

(Initial value **** ****) read only

Capture 2 data register high order

CAP2H (FFBDH)

7	6	5	4	3	2	1	0
CAP2 D15 (TBC16)	CAP2 D14 (TBC15)	CAP2 D13 (TBC14)	CAP2 D12 (TBC13)	CAP2 D11 (TBC12)	CAP2 D10 (TBC11)	CAP2 D9 (TBC10)	CAP2 D8 (TBC9)

(Initial value **** ****) read only

Capture control register

CAPCR (FFBEH)

7	6	5	4	3	2	1	0
CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS

(Initial value 0000 0000)

CAP2T (CFG)	Capture 2 trigger input status	0 : No trigger input 1 : Trigger input	read only
CAPCL	CAP1/CAP2 status clear	0 : – 1 : Clear (one-shot)	R/W

3.8 AC CLOCK INPUT CIRCUIT (ACCK)

AC clock input circuit (ACCK) is a digital noise canceler that samples the AC signal supplied from a home power source and transmits only those components that exceed the designated pulse width to a capture circuit.

The edge signal that is detected is inputted to capture 0 (CAP0) via a capture input control circuit (CAPIN). Measuring its cycle and discrimination of 50/60 Hz, etc. can be carried out easily by using capture function.

3.8.1 Circuit Structure

The AC clock input circuit (ACCK) comprises a 4-bit shift register that samples and shifts a signal level input from P33 (ACCK) terminal, a 4-bit comparator and RS flip-flop.

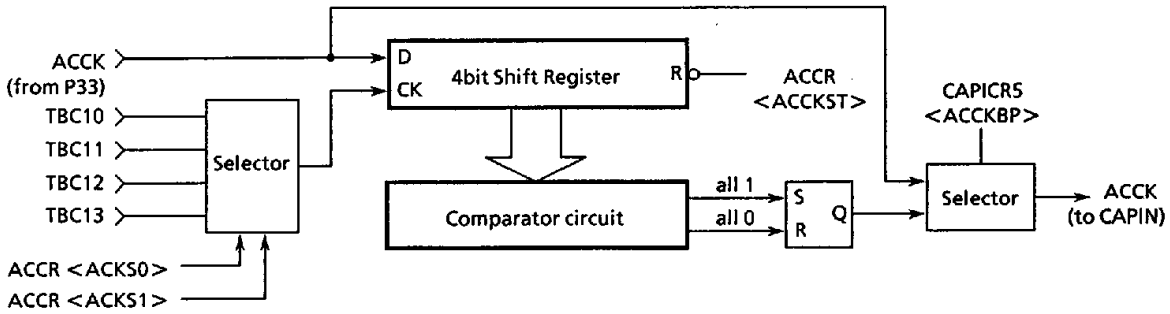


Fig. 3.8.1 Structure of AC Clock Input Circuit

3.8.2 Control Register

AC clock input control register

ACCR (F792H)

7	6	5	4	3	2	1	0
					ACCKST	ACKS1	ACKS0

(Initial value **** *000)

ACCKST	Start/stop AC clock sampling	0 : Stop 1 : Start	R/W
ACKS1	Selection of AC clock sampling rate	00 : TBC10 01 : TBC11 10 : TBC12 11 : TBC13	R/W
ACKS0			

Capture input control register 5

CAPICR5 (FFFAH)

7	6	5	4	3	2	1	0
		CTLSEL	RMTST	RMTP0	ACCKBP	RMTBP	CFGMCP

(Initial value **00 0000)

ACCKBP	AC Clock input control	0 : Sampling 1 : Bypass	R/W

3.8.3 Explanation of Operation

The signal input from ACCK (P33) terminal is sampled by the leading edge of the time base counter (TBC) output. When all of the output of the 4-bit shift register becomes "1", the RS flip-flop is set to "1". And when all values of the 4-bit shift register become "0", the RS flip-flop is reset to "0." The sampling/shift clock can be selected in one of TBC10-TBC13 using <ACKS1, ACKS0> of the AC clock control register (ACCR). In addition, the start/stop of sampling shift operations is controlled by ACCR <ACCKST>. By writing "0" to <ACCKST> the 4-bit shift register is cleared to all "0", the RS flip flop is resetted to "0" and shift operations stop.

The selection to sample or to bypass ACCK input is implemented using <ACCKBP> of capture input control register 5 (CAPICR5).

Table 3.8.1 shows the sampling clock rate and the minimum pulse width capable of being received as a regular input signal. Fig. 3.8.2 shows a timing chart for the AC clock input circuit.

<ACKS1, 0>	Sampling clock	Minimum pulse width regarded as a regular signal
00	TBC10 = fc / 2^{11}	2^{11} / fc × 4 (0.512 ms)
01	TBC11 = fc / 2^{12}	2^{12} / fc × 4 (1.024 ms)
10	TBC12 = fc / 2^{13}	2^{13} / fc × 4 (2.048 ms)
11	TBC13 = fc / 2^{14}	2^{14} / fc × 4 (4.096 ms)

Figures in brackets are when operating at 16MHz

Figure 3.8.1 Sampling Rate and Received Pulse Width (Minimum Value) for AC Clock Input Circuit

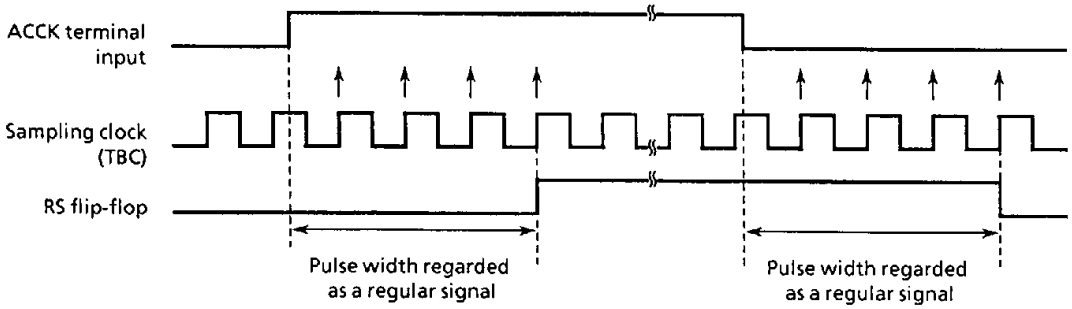


Figure 3.8.2 Timing Chart for AC Clock Input Circuit

3.9 REMOTE CONTROL SIGNAL INPUT CIRCUIT (RMTIN)

The remote control signal input circuit (RMTIN) consists of the loss recovery circuit and the noise cancellation circuit.

The leading edge and trailing edge detected by the RMTIN is inputted to the capture 0 (CAP0) via the capture input control circuit (CAPIN).

Width of the remote control signal can be measured by the CAP0.

3.9.1 Configuration

Each of the loss recovery circuit and the noise cancellation circuit consists of 4-bit binary up-counter, comparator and RS flip-flop.

Fig. 3.9.1 shows the configuration of the remote control signal input circuit.

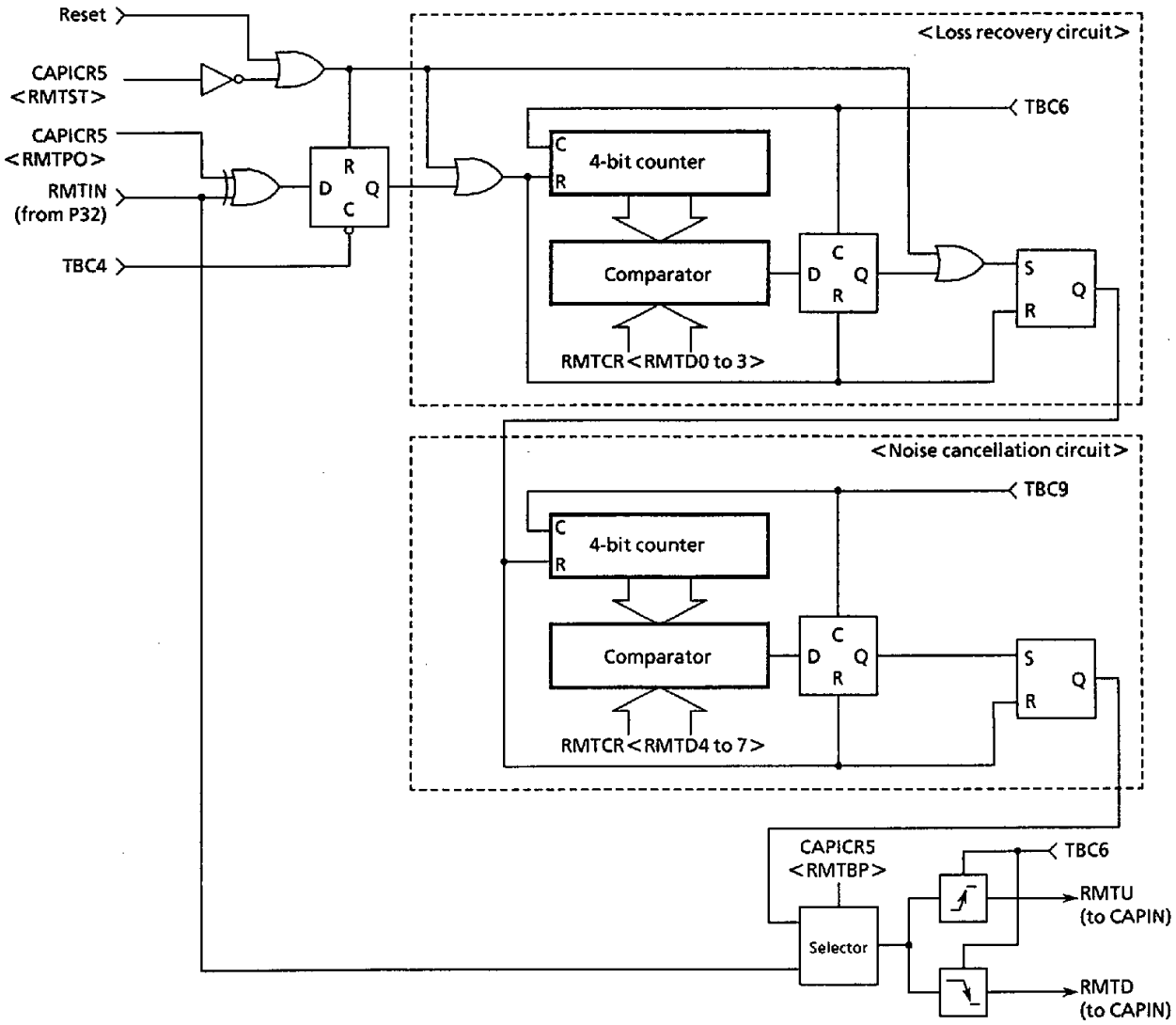


Fig. 3.9.1 Remote Control Signal Input Circuit

3.9.2 Control Registers

Remote control signal input control register

RMTCR (F795H)

7	6	5	4	3	2	1	0
RMTD7	RMTD6	RMTD5	RMTD4	RMTD3	RMTD2	RMTD1	RMTD0

(Initial value 0000 0000)

RMTD7 to RMTD4	Width of noise cancellation	Setting of comparative value of 4-bit counter (noise cancellation circuit)	R/W
RMTD3 to RMTD0	Width of loss recovery	Setting of comparative value of 4-bit counter (loss recovery circuit)	

Capture input control register 5

CAPICR5 (FFFAH)

7	6	5	4	3	2	1	0
		CTLSEL	RMTST	RMTPO	ACCKBP	RMTBP	CFGMCP

(Initial value **00 0000)

RMTST	Start/stop remote control signal input control	0 : Stop 1 : Start	R/W
RMTPO	Switching polarity of remote control signal input	0 : Positive 1 : Negative	
RMTBP	Bypass control for the remote control signal input	0 : Loss recovery and noise cancellation operation 1 : Bypass the loss recovery and noise cancellation circuit	

3.9.3 Operation of Remote Control Signal Input Circuit

(1) Control for the remote control signal input

The polarity of the remote control signal input from the RMTIN (P32) pin can be switched by <RMTPO> of the Capture input control resister 5 (CAPICR5). By setting <RMTPO> to "1" the input polarity can be reversed.

The remote control signal is sampled by the trailing edge of the TBC4 (2 ms when operating at 16 MHz) of the Time base counter (TBC) output.

Hereinafter, the operation in case of <RMTPO> = 0 (positive polarity) will be explained.

(2) Operation of the loss recovery circuit

In case that high-active remote control signal is received, the loss recovery circuit recovers negative polarity loss pulse which width is less than that is set in the Remote control signal input control register RMTCR <RMTD3 to RMTD0>.

The 4-bit counter counts TBC6 (8 μs when operating at 16 MHz) of the Time base counter output. So, <RMTD3 to RMTD0> should be set a value equivalent to width of loss pulse which is planned to be recovered. In case of receiving negative pulse which width is more than setting value in the RMTCR <RMTD3 to RMTD0>, the remote control signal input circuit judges that the trailing edge of negative pulse was trailing edge of remote control signal and outputs the "RMTD" signal to capture input control circuit (CAPIN).

(3) Operation of the noise cancellation circuit

In case that high-active remote control signal is received, the noise cancellation circuit cancels positive polarity pulse which width is less than that is set in the Remote control signal input control register RMTCR <RMTD7 to RMTD4>.

The 4-bit counter counts TBC9 (64 μs when operating at 16 MHz) of the Time base counter output. So, <RMTD7 to RMTD4> should be set a value equivalent to width of positive polarity pulse which is planned to be canceled. In case of receiving positive pulse which width is more than setting value in the RMTCR <RMTD7 to RMTD4>, the remote control signal input circuit judges that the leading edge of positive pulse was leading edge of remote control signal and output the "RMTU" signal to capture input control circuit (CAPIN).

(4) Measuring the pulse width of remote control signal

"RMTU" signal (leading edge of the remote control signal) and "RMTD" signal (trailing edge of the remote control signal) are inputted to the Capture 0 (CAP0) via the Capture input control circuit (CAPIN). The width of remote control signal can be calculated by software which uses timing data of RMTU and RMTD.

In case of setting data 0000H to the RMTCR <RMTD3 to 0> or <RMTD7 to RMTD4>, the Remote control signal input circuit doesn't perform a loss recovery or noise cancellation operation, and when CAPICR5 <RMTBP> is set to "1", the remote control signal inputted to the Capture input control circuit (CAPIN) is by-passed the Loss recovery and Noise cancellation circuit.

Fig. 3.9.2 shows the operational timing chart of the remote control signal input circuit.

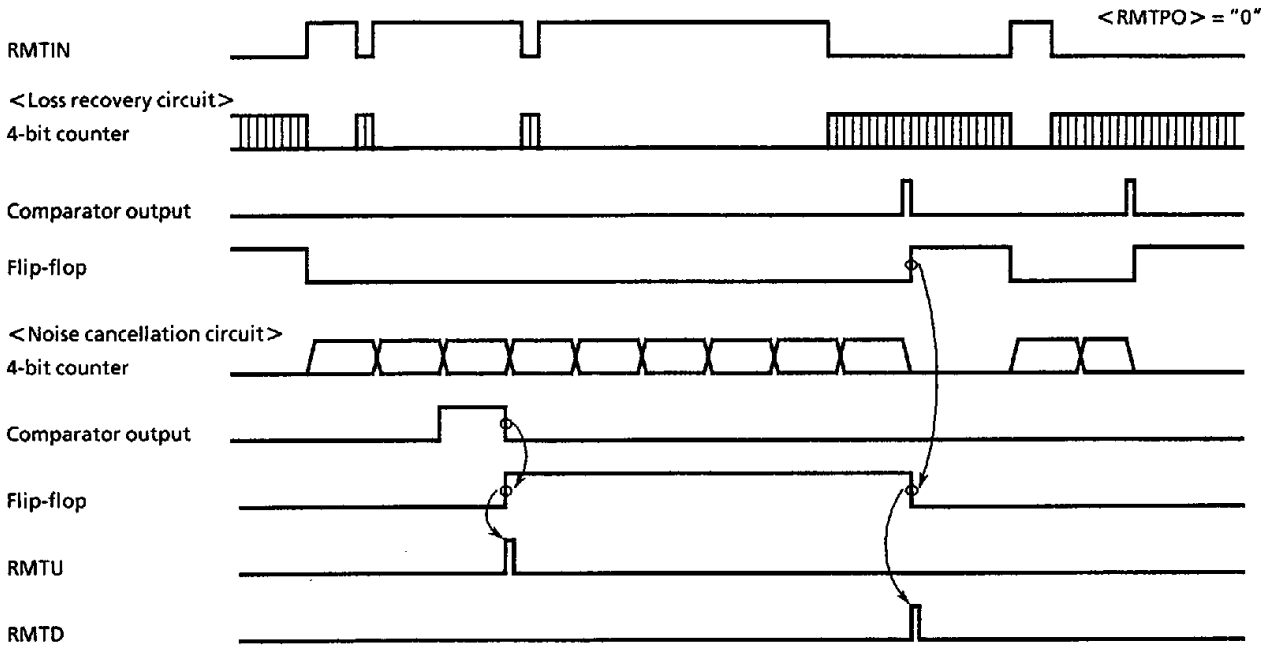


Fig. 3.9.2 Remote Control Signal Input Circuit Timing Chart

3.10 TIMING PULSE GENERATOR (TPG)

In order to generate the various timing pulses necessary for VTR system control, the TMP90CR74A has a timing pulse generator (TPG0) with 22-bit 4-stage FIFO buffer and a 20-bit timing pulse generator (TPG1).

The TPG0 and TPG1 can output the timing pulse synchronized with the time base counter (TBC). Their resolution for both TPG0 and TPG1 is 500 ns (when operating at 16 MHz).

3.10.1 Timing Pulse Generator 0 (TPG0)

(1) Configuration

The TPG0, as shown in Fig. 3.10.1, is composed of 22-bit 4-stage FIFO data register (16-bit timing data + 6-bit output data), 16-bit comparator, 6-bit output data buffer and FIFO control circuit.

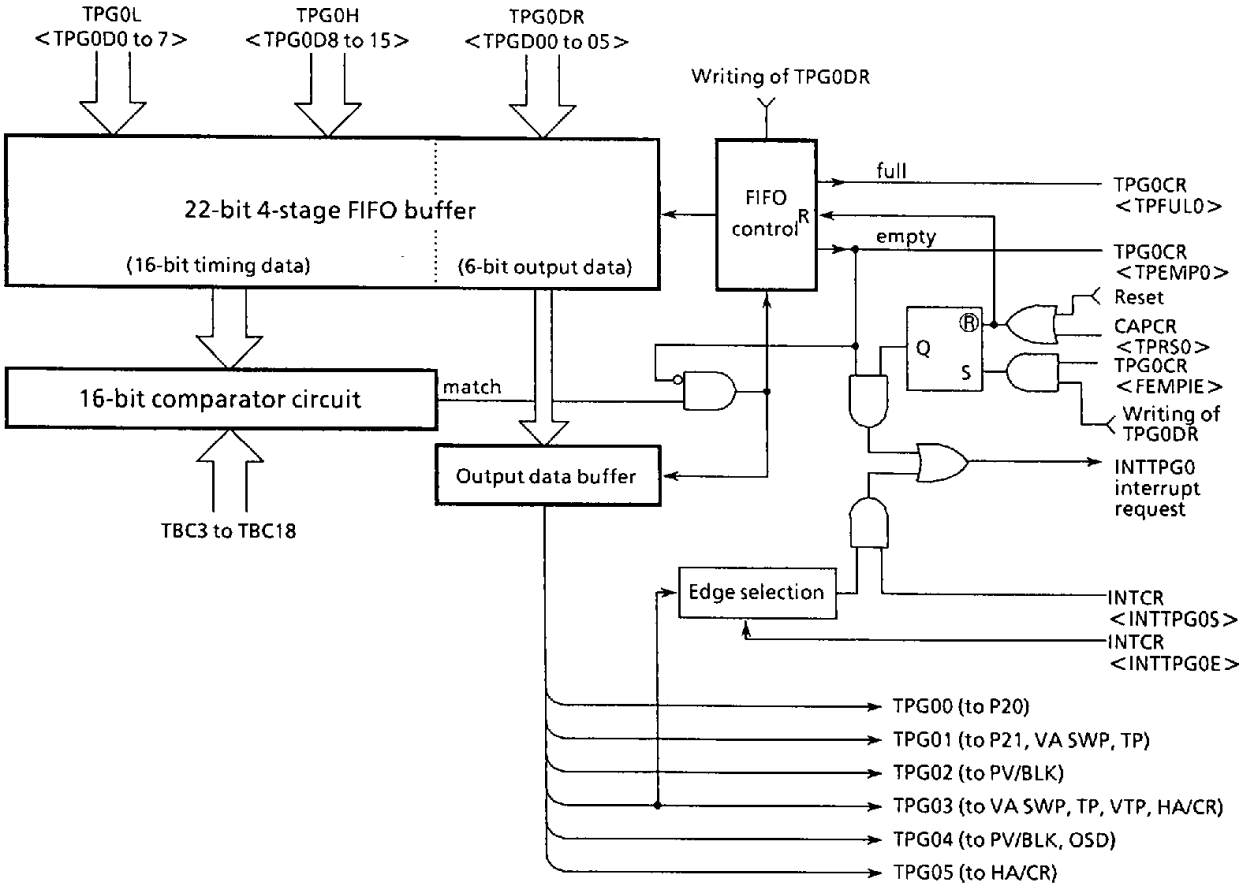


Fig. 3.10.1 Configuration of Timing Pulse Generator 0 (TPG0)

(2) Operation

① 22-bit 4-stage FIFO buffer

This is a 22-bit data register which is composed of 16-bit timing data and 6-bit output data. As this register has a 4-stage FIFO structure, the first written timing data and output data are transferred first to the comparator and output data register.

Set to the lower timing data register (TPG0L), the higher timing data register (TPG0H) and the output data register (TPG0DR) in this order. The FIFO address is incremented by writing of TPG0DR.

6-bit output data is transferred to the output data buffer when 16-bit timing data matches the value of TBC3 to TBC18. And they become the TPG00 to TPG05.

② 16-bit comparator

When the set data of the TPG0L and TPG0H matches the value of TBC3 to TBC18, the comparator outputs the match signal. The value of TPG0DR is transferred to output data buffer and the FIFO address is incremented by the match signal.

③ Output data buffer

The data set in the output data register (TPG0DR) is latched by the match signal from the 16-bit comparator, and TPG00 to TPG05 outputs are changed. When resetting, this buffer is cleared to "0" and TPG00 to TPG05 outputs become "0".

④ FIFO control circuit

The FIFO control circuit controls the 22-bit 4-stage FIFO buffer and has a status flag to monitor the FIFO address.

The current number of retained data can be verified by reading out the FIFO status flags <TPF01, TPF00> of the TPG0 control register (TPG0CR). In case that the value of the FIFO status flag is "00", the FIFO empty flag <TPEMP0> is set to "1" when retained data is nothing and the FIFO full flag <TPFUL0> is set to "1" when retained data are 4 words. And, writing data to the FIFO buffer is disabled while the <TPFUL0> is set to "1". The contents of the FIFO status flags is varied each time the match signal is outputted from the comparator. The contents of the FIFO status flags is cleared to "00" by resetting. In addition, the FIFO address can be cleared by writing "1" to <TPRS0> of the capture control register (CAPCR).

⑤ Timing pulse generator 0 interrupt (INTTPG0)

When the contents of the FIFO buffer becomes empty, an INTTPG0 (empty) interrupt to request the writing of the next data is generated. The INTTPG0 (empty) interrupt request can be controlled by TPG0CR <FEMPIE> and CAPCR <TPRS0>. By setting <FEMPIE> to "1", INTTPG0 (empty) interrupt request is enabled by writing of TPG0 output data register (TPG0DR). And by writing "1" to CAPCR <TPRS0>, it can be disabled (in this case FIFO address will also be cleared).

In addition, INTTPG0 (TPG03) interrupt request can be generated synchronized with the leading edge or trailing edge of TPG03. Either leading or trailing edge of TPG03 can be selected by <INTTPG0E> of interrupt control register (INTCR). To enable or disable INTTPG0 (TPG03) interrupt request can be selected using INTCR <INTTPG0S>.

INTTPG0 interrupt request is generated as logical-OR with INTTPG0 (empty) interrupt request and INTTPG0 (TPG03) interrupt request.

(3) Control Register

TPG0 control register

TPG0CR (FFEAH)

7	6	5	4	3	2	1	0
			FEMPIE	TPFUL0	TPEMP0	TPF01	TPF00

(Initial value ***0 0100)

FEMPIE	Enabling of INTTPG0 (empty) interrupt request	0 : – 1 : Enable	write only
TPFUL0	TPG0 FIFO full flag	0 : – 1 : FIFO full	read only
TPEMP0	TPG0 FIFO empty flag	0 : – 1 : FIFO empty	
TPF01 TPF00	TPG0 FIFO status flag	00 : Empty or full 01 : Retained data is 1 word 10 : Retained data is 2 words 11 : Retained data is 3 words	

TPG0 lower timing data register

TPG0L (FFEBH)

7	6	5	4	3	2	1	0
TPG0D7	TPG0D6	TPG0D5	TPG0D4	TPG0D3	TPG0D2	TPG0D1	TPG0D0

(Initial value **** ****) Write only

TPG0 higher timing data register

TPG0H (FFECH)

7	6	5	4	3	2	1	0
TPG0 D15	TPG0 D14	TPG0 D13	TPG0 D12	TPG0 D11	TPG0 D10	TPG0 D9	TPG0 D8

(Initial value **** ****) Write only

TPG0 output data register

TPG0DR (FFEDH)

7	6	5	4	3	2	1	0
		TPGD05	TPGD04	TPGD03	TPGD02	TPGD01	TPGD00

(Initial value **** ****) Write only

Capture control register

CAPCR (FFBEH)

7	6	5	4	3	2	1	0
CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS

TPRS0	Clearing of FIFO address and disabling of INTTPG0 (empty) interrupt request	0 : – 1 : Clearing of FIFO address and disabling of INTTPG0 (empty) interrupt request (one-shot)	R/W

Interrupt control register

INTCR (F78FH)

7	6	5	4	3	2	1	0
		CLKCK	$\overline{CLOE}$	INTT PG0E	INTT PG0S	T3ADS	T0DIRS

(Initial value **00 0000)

INTTPG0E	INTTPG0 (TPG03) interrupt Edge selection	0 : Leading edge of TPG03 1 : Trailing edge of TPG03	R/W
INTTPG0S	Enabling/disenabling of INTTPG0 (TPG03) interrupt request	0 : Disable 1 : Enable	

(4) Output of timing pulse generator 0

① TPG00
TPG00 is outputted from P20 (TPG00) pin.
(Refer to 3.21.3 P2 Port.)

② TPG01
TPG01 can be used as AFF (audio head switching) signal.
TPG01 is outputted from P21 (TPG01) pin. And TPG01 controls VASWP output and TP0 to TP3 output.
(Refer to 3.21.3 P2 Port, 3.13.4 Control of VASWP Output and 3.10.3 Timing Pulse Output.)

③ TPG02
TPG02 controls the pseudo synchronizing signal output (PV).
(Refer to 3.15 Pseudo Synchronizing Signal Output Circuit.)

④ TPG03
TPG03 can be used as DFF (cylinder head switching) signal.
TPG03 controls VASWP output, TP0 to TP3 output, VTP0 to VTP4 output, HA output and CR output.
(Refer to 3.13 Head Amplifier/Color Rotary Control Circuits and 3.10.3 Timing Pulse Output.)

⑤ TPG04
TPG04 controls the pseudo synchronizing signal output (PV).
(Refer to 3.15 Pseudo Synchronizing Signal Output Circuit and 3.16 On-screen Display Circuit.

⑥ TPG05
TPG05 controls HA/CR output.
(Refer to 3.13 Head Amplifier (HA) /Color Rotary (CR) Control Circuit.

3.10.2 Timing Pulse Generator (TPG1)

(1) Configuration

TPG1 consist of a 20-bit data register (16-bit timing data + 4-bit output data), 16-bit comparator and 4-bit output data buffer.

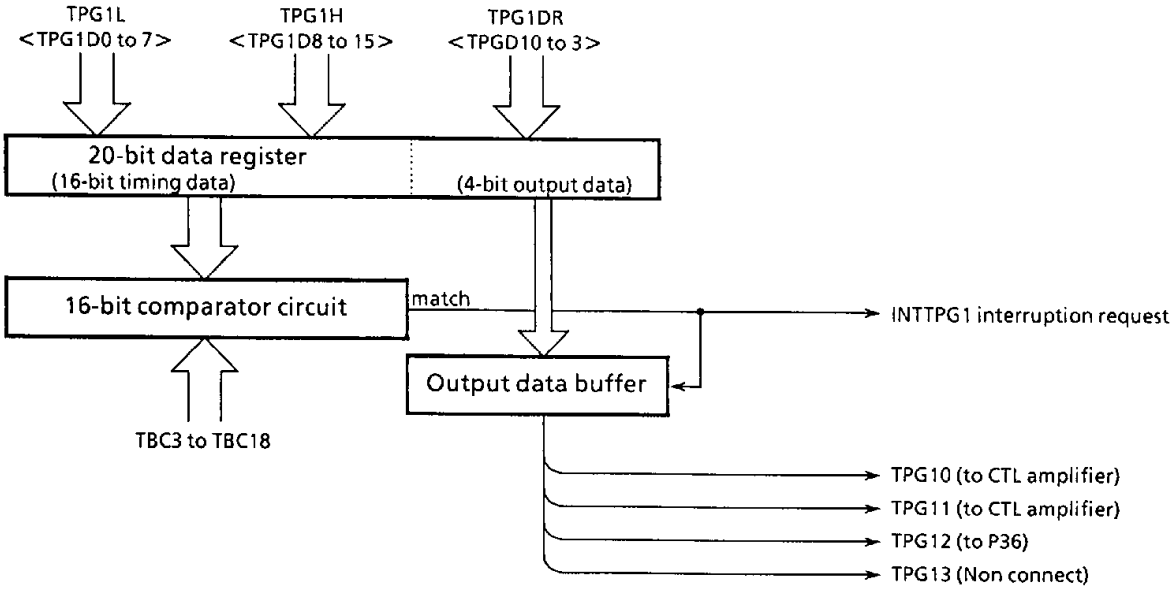


Fig. 3.10.2 Configuration of Timing Pulse Generator 1 (TPG1)

(2) Operation

① 20-bit data register

This is a 20-bit data register which is composed of 16-bit timing data and 4-bit output data. Set to the lower timing data register (TPG1L), higher timing data register (TPG1H), and the output data register (TPG0DR). 4-bit output data is transferred to the output data buffer when 16-bit timing data matches the value of TBC3 to TBC18. And they become the TPG10 to TPG13.

② 16-bit comparator

When the set data of the TPG1L and TPG1H matches the value of TBC3 to TBC18, the comparator outputs the match signal. The value of the TPG1DR is transferred to output data buffer and INTTPG1 interrupt request is generated by the match signal.

③ Output data buffer

The data set in the output data register (TPG1DR) is latched by the match signal from the 16-bit comparator, and TPG00 to TPG05 are outputted. When resetting, this buffer is cleared to "0" and TPG10 to TPG13 output become "0".

(3) Control register

TPG1 lower timing data register

TPG1L (FFEEH)	7	6	5	4	3	2	1	0			
	TPG1D7	TPG1D6	TPG1D5	TPG1D4	TPG1D3	TPG1D2	TPG1D1	TPG1D0	(Initial value	0000 0000)	Write only

TPG1 higher timing data register

TPG1H (FFEFH)	7	6	5	4	3	2	1	0			
	TPG1D15	TPG1D14	TPG1D13	TPG1D12	TPG1D11	TPG1D10	TPG1D9	TPG1D8	(Initial value	0000 0000)	Write only

TPG1 output data register

TPG1DR (FFF0H)	7	6	5	4	3	2	1	0			
					TPGD13	TPGD12	TPGD11	TPGD10	(Initial value	**** 0000)	Write only

(4) Output of timing pulse generator 1

① TPG10

TPG10 controls the recording amplifier for CTL signal.
(Refer to 3.20 Servo Control Amplifier.)

② TPG11

TPG11 controls the recording amplifier for CTL signal.
(Refer to 3.20 Servo Control Amplifier.)

③ TPG12

TPG12 can be output from TPG12 (P36) pin.
(Refer to 3.21.4 P3 Port.)

3.10.3 Timing pulse output (TP/VTP)

Timing pulse generator 0 (TPG0) outputs TPG01 and TPG03 can be used as AFF (audio head switch) and DFF (cylinder head switch) signals, and can be output from the VASWP terminal (refer to 3.13.4 Control of VASWP Output).

In addition, timing pulses synchronized with the AFF signal or DFF signal can be output from TP0 to TP3 pins, and timing pulses synchronized with the DFF signal can be output from VTP0 to VTP4 pins.

Table 3.10.1 shows timing pulse outputs and its output pins.

Table 3.10.1 Timing Pulse Output and its output pins

Timing Pulse Output	output pins
TP0	P20 (TPG00)
TP1	P21 (TPG01)
TP2	P24 (TI3)
TP3	P36 (TI2 / TO3)
VTP0	P52 (SDA0 / RXD2)
VTP1	P53 (SCL0 / SCLK2)
VTP2	P54 (TXD2)
VTP3	P22 (CR)
VTP4	P23 (HA)

(Refer to 3.21.3 P2 Port and 3.21.6 P5 Port concerning configuration of timing pulse output circuit and explanation of operation.)

3.11 PULSE WIDTH MODULATION OUTPUT (PWM)

The TMP90CR74A has four pulse width modulation (PWM) output channels. There are 2 channels of 12-bit resolution (PWM0/PWM1), 1 channel of 8-bit resolution (PWM2), and 1 channel of 14-bit resolution (PWM3). These can be used for AFC (Automatic frequency control) and APC (Automatic phase control) outputs of servo control, Voltage synthesize tunning control, and other apprication with an external low-pass filter.

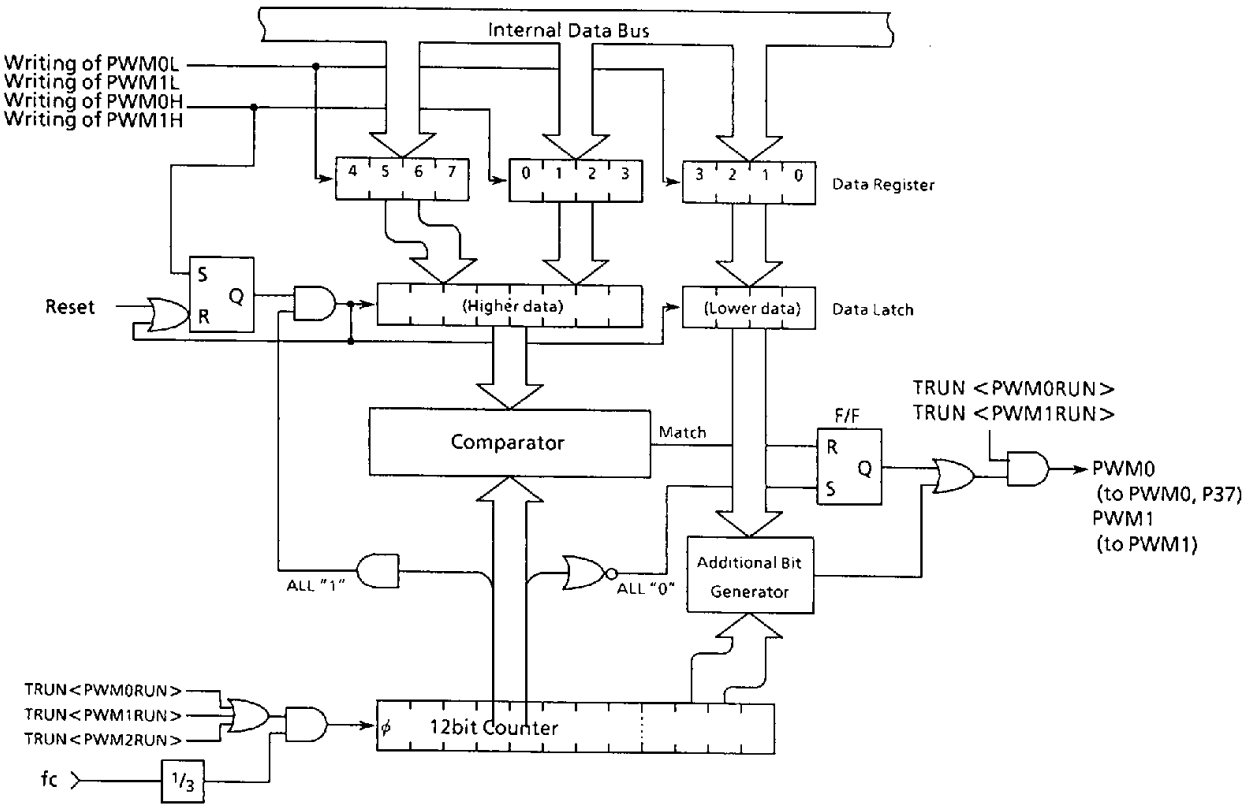
3.11.1 12-bit Pulse Width Modulation (PWM0, PWM1)

PWM0 and PWM1 are controlled by data register (PWM0L/PWM0H and PWM1L/PWM1H), PWM control register (PWMCR) and timer start register (TRUN). By setting PWMCR <PWM01M>, the carrier frequency can be selected from 20.83 kHz or 41.67 kHz (When operating at 16 MHz).

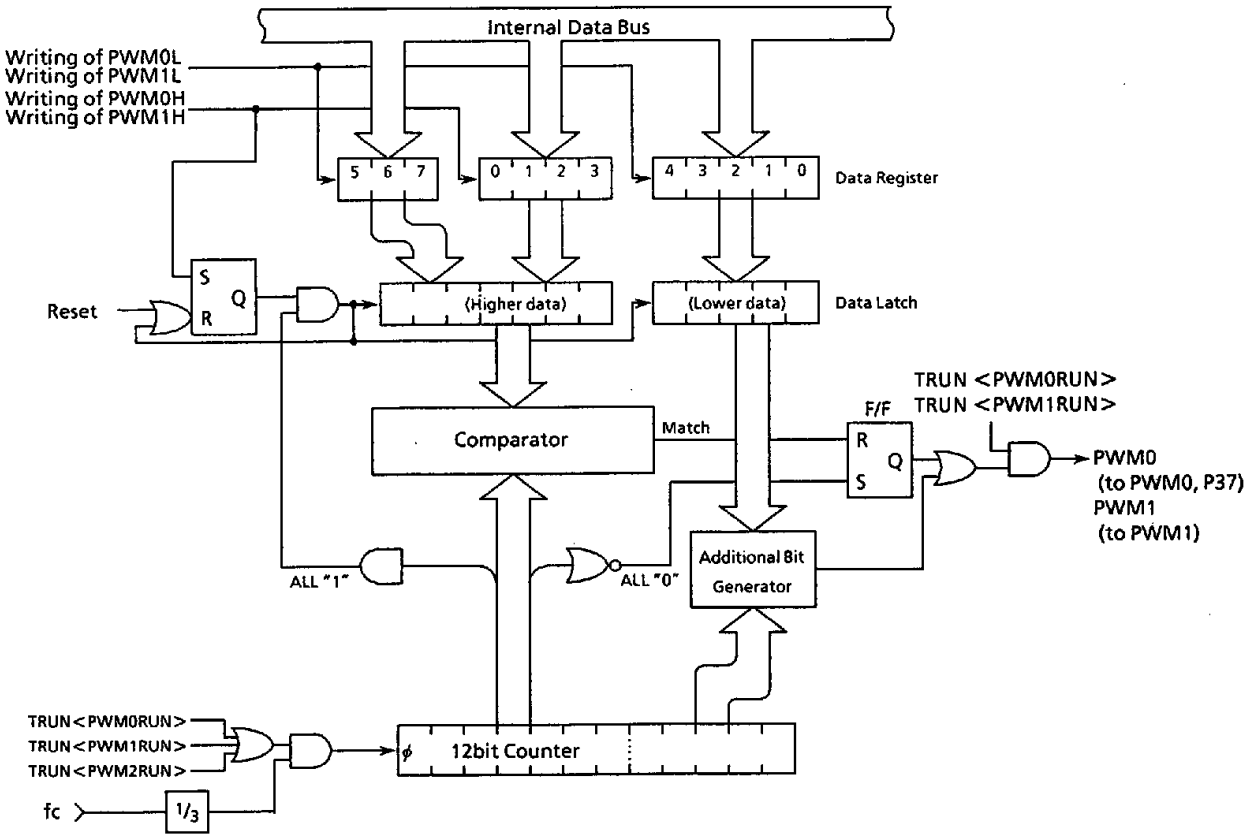
Phase difference with PWM0 and PWM1 is half cycle (180°). Further, the PWM0 output is connected to the CAPFER (P37) pin, generating a timing pulse synchronized to PWM0 is possible. (Refer to Section 3.21.4 P3 Port.)

(1) Configuration

Figure 3.11.1 shows the configuration of the 12-bit PWM. They show in case that <PWM01M> is set to "0" or "1".



(a) Carrier frequency is 20.83 kHz (PWMCR <PWM01M> = 0)



(b) Carrier frequency is 41.67 kHz (PWMCR <PWM01M> = 1)

Figure 3.11.1 12-bit pulse width modulation output (PWM0/PWM1)

(2) Control of PWM output

The PWM0 and PWM1 outputs are 12-bit resolution pulse outputs whose one cycle is TM = 2^{12} /(fc/3) [s]. The carrier frequency can be selected from $T_S = T_M/16$ [s] (20.83 kHz when operating at 16 MHz) or $T_S = T_M/32$ [s] (41.67 kHz when operating at 16 MHz) by the PWMCR <PWM01M>. The data register used to set the pulse width are PWM0L, PWM0H and PWM1L, PWM1H.

The order of writing to the data registers is the Lower data register (PWM0L, PWM1L) and the Higher data register (PWM0H, PWM1H). After writing to the higher data register, the data is transferred to the Data Latch immediately before the next TM cycle. Supposing that the higher data in the data latch is 'n' and the lower data is 'm', then the pulse width is $n \times t_0$ (t_0 = 1/ (fc/3)) [s], and additional pulse (t0 [s]) is added to 'm' spaces in the carrier pulse that is outputted during one T_M cycle. Therefore, the carrier pulse width included with an additional pulse becomes (n + 1) t_0 [s].

PWM0 and PWM1 are triggered to start outputting by setting the TRUN <PWM0RUN and PWM1RUN> to "1". Phase difference with PWM0 and PWM1 is half cycle (180°).

Figure 3.11.2 shows a timing chart of the 12-bit pulse width modulation outputs.

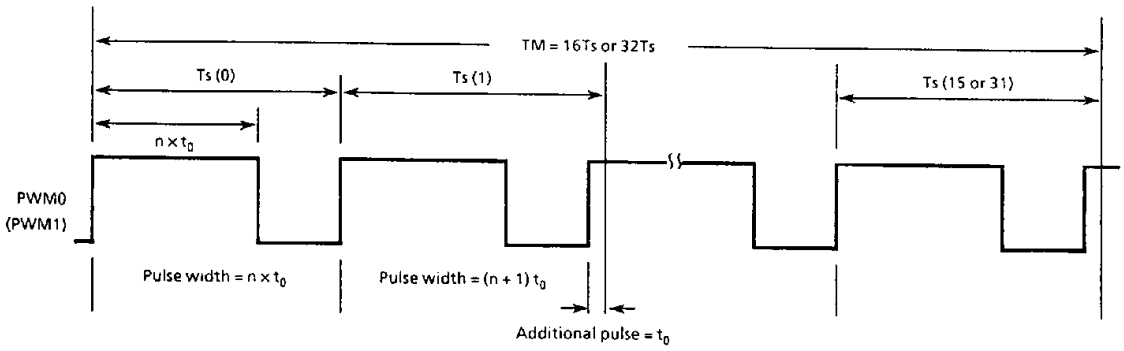


Figure 3.11.2 Timing chart of the 12-bit pulse width modulation outputs

If all bits in the data registers are written "1", the PWM0/PWM1 output negative pulse which width is t0 [s] every TM cycle.

(3) Control Register

PWM 0 Lower Data Register

PWM0L (FFD5H)

7	6	5	4	3	2	1	0
PWM 0D7	PWM 0D6	PWM 0D5	PWM 0D4	PWM 0D3	PWM 0D2	PWM 0D1	PWM 0D0

(Initial value **** ****) Write only

PWM 0 Higher Data Register

PWM0H (FFD6H)

7	6	5	4	3	2	1	0
				PWM 0D11	PWM 0D10	PWM 0D9	PWM 0D8

(Initial value **** ****) Write only

PWM 1 Lower Data Register

PWM1L (FFD7H)

7	6	5	4	3	2	1	0
PWM 1D7	PWM 1D6	PWM 1D5	PWM 1D4	PWM 1D3	PWM 1D2	PWM 1D1	PWM 1D0

(Initial value **** ****) Write only

PWM 1 Higher Data Register

PWM1H (FFD8H)

7	6	5	4	3	2	1	0
				PWM 1D11	PWM 1D10	PWM 1D9	PWM 1D8

(Initial value **** ****) Write only

Timer Start Control Register

TRUN (FFD4H)

7	6	5	4	3	2	1	0
PWM3 RUN	T3RUN	PWM1 RUN	PWM0 RUN	PWM2 RUN	T2RUN	T1RUN	T0RUN

(Initial value 0000 0000)

PWM1RUN	PWM1 Start / Stop	0 : Stop 1 : Start	R/W
PWM0RUN	PWM0 Start / Stop	0 : Stop 1 : Start	

PWM Control Register

PWMCR (F793H)

7	6	5	4	3	2	1	0
	PWM 01M	CFRT RGS	SYNCPO	PWMSEL	PWMPO2	PWMPO1	PWM PO0

(Initial value *000 0000)

PWM01M	PWM0,1 Carrier Selection	0 : Ts = 20.83 kHz (at fc = 16 [MHz]) 1 : Ts = 41.67 kHz (at fc = 16 [MHz])	R/W
PWMPO1	PWM1 Output polarity selection	0 : Positive 1 : Inverted	
PWMPO0	PWM0 Output polarity selection	0 : Positive 1 : Inverted	

Open-drain control register 1

ODMCR1 (F789H)

7	6	5	4	3	2	1	0
PWM1OC	PWM0OC	P37OC	P24OC	P23OC	P22OC	P21OC	P20OC

(Initial value 0000 0000)

PWM1OC	PWM1 open-drain control	0 : Push-pull output 1 : Open-drain output	R/W
PWM0OC	PWM0 open-drain control	0 : Push-pull output 1 : Open-drain output	

(4) PWM output ports

The PWM0 output is driven from the PWM0 pin and the PWM1 output is driven from the PWM1 pin. Figure 3.11.3 shows the configuration of the PWM0 and PWM1 output ports.

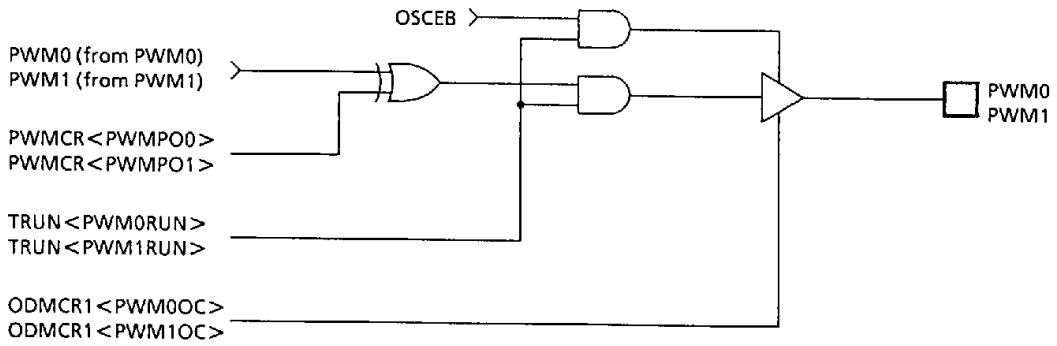


Figure 3.11.3 PWM0 and PWM1 output ports

The PWM0 and PWM1 pins are used exclusively for 12-bit pulse width modulated outputs. Their output buffers are enabled by setting the timer start control register (TRUN) <PWM0RUN> and <PWM1RUN> to "1" respectively, Furthermore, their outputs can be switched between push-pull output or N-channel open-drain output by using the open-drain control register 1 (ODMCR1) <PWM0OC> and <PWM1OC>.

In addition, the polarity of the PWM output can be inverted by setting the PWM control register (PWMCR) <PWMPO0> and <PWMPO1> to "1".

3.11.2 8-bit Pulse Width Modulation (PWM2)

PWM2 is controlled by the data register (PWM2DR) and timer start control register (TRUN).

The PWM2 output is driven from the P74 (PWM3) pin. The P74 pin is shared between PWM2 and PWM3 output. (Refer to Section 3.21.8 P7 Port.)

(1) Configuration

Figure 3.11.4 shows the configuration of the 8-bit PWM.

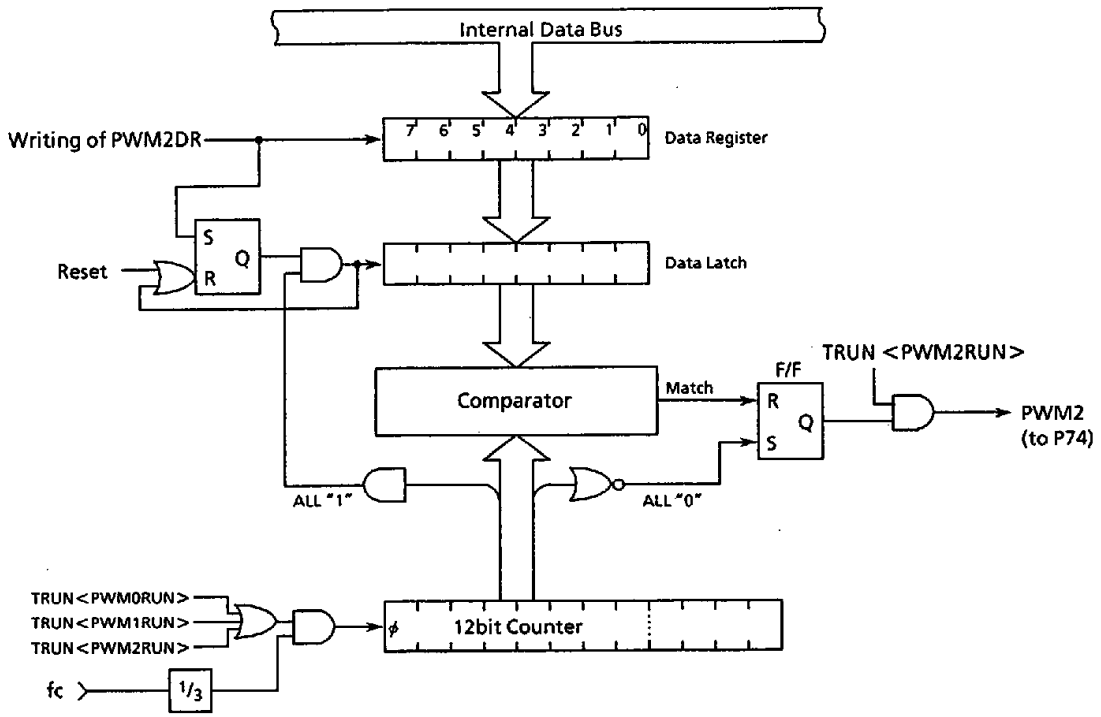


Figure 3.11.4 8-bit pulse width modulation output (PWM2)

(2) Control of PWM output

The PWM2 output is an 8-bit resolution pulse output whose one cycle is TM = 2^8/ (fc/3)) [s]. Supposing that the value set in the PWM2 data register (PWM2DR) is 'n', the pulse whose width is n x t_0 (t_0 = 1/ (fc/3)) [s] in the TM cycle is outputted. The 12-bit counter is shared between PWM2 and PWM0/PWM1. When all of the lower 8 bits become "1", the value written to the data register is transferred to the data latch.

PWM2 is triggred to start outputting by setting the TRUN <PWM2RUN> to "1".

Figure 3.11.5 shows a timing chart of the 8-bit pulse width modulation output.

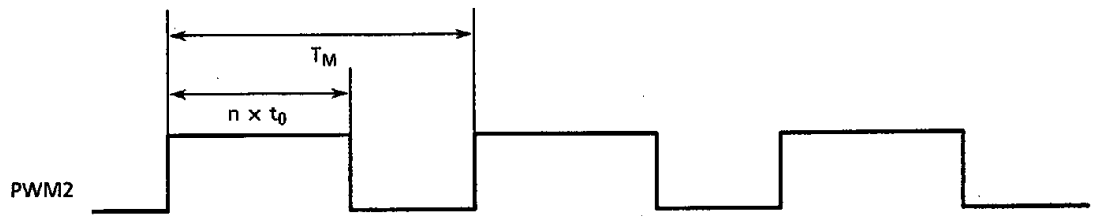


Figure 3.11.5 Timing chart of 8-bit pulse width modulation output

If all bits in the data registers are written "1", the PWM2 outputs negative pulse which width is t_0 [s] every 16 TM cycles.

(3) Control register

PWM 2 Data Register

PWM2DR (FFD9H)

7	6	5	4	3	2	1	0
PWM 2D7	PWM 2D6	PWM 2D5	PWM 2D4	PWM 2D3	PWM 2D2	PWM 2D1	PWM 2D0

(Initial value **** ****) Write only

Timer Start Control Register

TRUN (FFD4H)

7	6	5	4	3	2	1	0
PWM3 RUN	T3RUN	PWM1 RUN	PWM0 RUN	PWM2 RUN	T2RUN	T1RUN	T0RUN

(Initial value 0000 0000)

PWM2RUN	PWM2 Start / Stop	0 : Stop 1 : Start	R/W

PWM control register

PWMCR (F793H)

7	6	5	4	3	2	1	0
	PWM 01M	CFRT RGS	SYNCPO	PWMSEL	PWMPO2	PWMPO1	PWMPO0

(Initial value *000 0000)

PWMSEL	Switch between PWM2 and PWM3 outputs.	0 : PWM2 is outputted from P74 pin. 1 : PWM3 is outputted from P74 pin.	R/W
PWMPO2	Switch over PWM2/PWM3 output polarity.	0 : Positive 1 : Inverted	

Open-drain control register 2

ODMCR2 (F78AH)

7	6	5	4	3	2	1	0
			P74OC	P56OC	P55OC	P53OC	P52OC

(Initial value ***0 0000)

P74OC	P74 open-drain control	0 : Push-pull output 1 : Open-drain output	R/W

(4) PWM2 output

The PWM2 output is driven from the P74 pin. (Refer to Section 3.21.8 P7 Port.) The P74 pin is shared between PWM2 and PWM3 output. Which is outputted from this pin, PWM2 or PWM3, is selected by using the PWM control register (PWMCR) <PWMSEL>. The polarity of the PWM2 (PWM3) output can be inverted by setting the PWMCR <PWMPO2> to "1".

Furthermore, the P74 output buffer can be switched between push-pull output and N-channel open-drain output by using the open-drain control register 2 (ODMCR2) <P74OC>.

3.11.3 14-bit Pulse Width Modulation (PWM3)

PWM3 is controlled by the data registers (PWM3L/PWM3H) and timer start control register (TRUN).

The PWM3 output is driven from the P74 (PWM2) pin. The P74 pin is shared between PWM2 and PWM3 output.

(Refer to Section 3.21.8 P7 Port.)

(1) Configuration

Figure 3.11.6 shows the configuration of the 14-bit PWM.

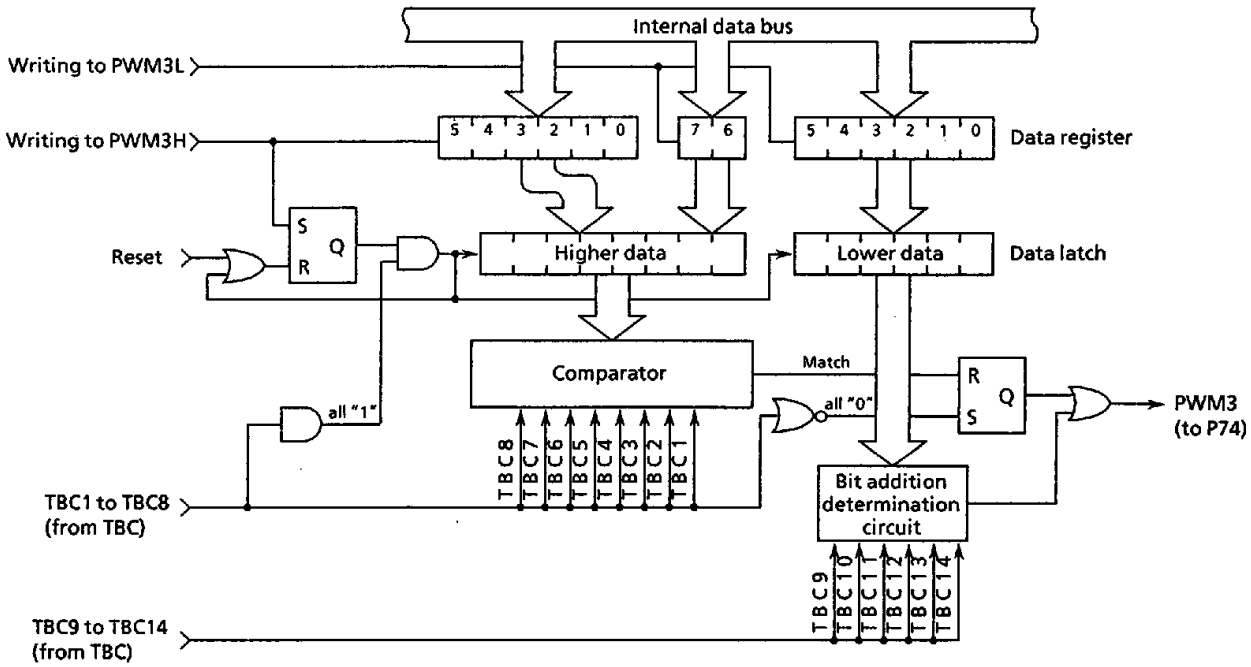


Figure 3.11.6 14-bit pulse width modulation output

(2) Control of PWM output

The PWM3 output is a 14-bit resolution pulse output whose one cycle is $T_M = 2^{14}/(fc/2)$ [s]. The carrier frequency is $T_S = T_M/64$ [s]. The data register used to set the pulse width is PWM3L and PWM3H.

The order of writing to the data registers is the lower data register (PWM3L) and the higher data register (PWM3H). After writing to the higher data register, the data is transferred to the Data Latch immediately before the next TM cycle. Supposing that the higher data in the data latch is 'n' and the lower data is 'm', then the pulse width is $n \times t_0$ ($t_0 = 1/(fc/2)$) [s], and additional pulse (t0 [s]) is added to 'm' spaces in the carrier pulse that is outputted during one T_M cycle. Therefore, the carrier pulse width included with an additional pulse becomes $(n + 1)\ t_0$ [s]. PWM3 is triggered to start outputting by setting the TRUN <PWM3RUN> to "1".

Figure 3.11.7 shows a timing chart of the 14-bit pulse width modulation output.

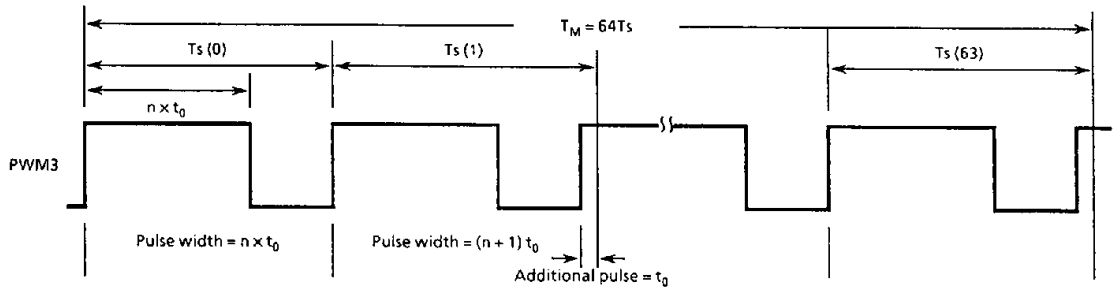


Figure 3.11.7 Timing chart of 14-bit pulse width modulation output

(3) Control register

PWM3 Lower Data Register

PWM3L (F788H)

7	6	5	4	3	2	1	0
PWM 3D7	PWM 3D6	PWM 3D5	PWM 3D4	PWM 3D3	PWM 3D2	PWM 3D1	PWM 3D0

(Initial value **** ****) Write only

PWM3 Higher Data Register

PWM3H (F78CH)

7	6	5	4	3	2	1	0
		PWM 3D13	PWM 3D12	PWM 3D11	PWM 3D10	PWM 3D9	PWM 3D8

(Initial value **** ****) Write only

Timer Start Control Register

TRUN (FFD4H)

7	6	5	4	3	2	1	0
PWM3 RUN	T3RUN	PWM1 RUN	PWM0 RUN	PWM2 RUN	T2RUN	T1RUN	T0RUN

(Initial value 0000 0000)

PWM3RUN	PWM3 Start / Stop	0 : Stop 1 : Start	R/W

PWM control register

PWMCR (F793H)

7	6	5	4	3	2	1	0
	PWM 01M	CFRT RGS	SYN CPO	PWM SEL	PWM PO2	PWM PO1	PWM PO0

(Initial value *000 0000)

PWMSEL	Switch between PWM2 and PWM3 outputs.	0 : PWM2 is outputted from P74 pin. 1 : PWM3 is outputted from P74 pin.	R/W
PWMPO2	Switch over PWM2/PWM3 output polarity.	0 : Positive 1 : Inverted	

Open-drain control register 2

ODMCR (F78AH)

7	6	5	4	3	2	1	0
			P74OC	P56OC	P55OC	P53OC	P52OC

(Initial value ***0 0000)

P74OC	P74 open-drain control	0 : Push-pull output 1 : Open-drain output	R/W

(4) PWM3 output

The PWM3 output is driven from the P74 pin. (Refer to Section 3.21.8 P7 Port.) The P74 pin is shared between PWM2 and PWM3 output. Which is outputted from this pin, PWM2 or PWM3, is selected by using the PWM control register (PWMCR) <PWMSEL>. The polarity of the PWM3 (PWM2) output can be inverted by setting the PWMCR <PWMPO2> to "1".

Furthermore, the P74 output buffer can be switched between push-pull output and N-channel open-drain output by using the open-drain control register 2 (ODMCR2) <P74OC>.

3.12 VISS / VASS DETECTOR (VIVA)

This circuit is to support the Video Index Search System (VISS) and Video Address Search System (VASS) for VHS VCR. By using this circuit, the duty of control signal (CTL) recorded on video tapes is can be measured and the VISS code can be detected. Further, the address code of VASS can be read out.

3.12.1 Configuration

VISS / VASS detector consists of the CTL duty discrimination circuit, VISS detection circuit, VASS header detection circuit and 16-bit address code register.

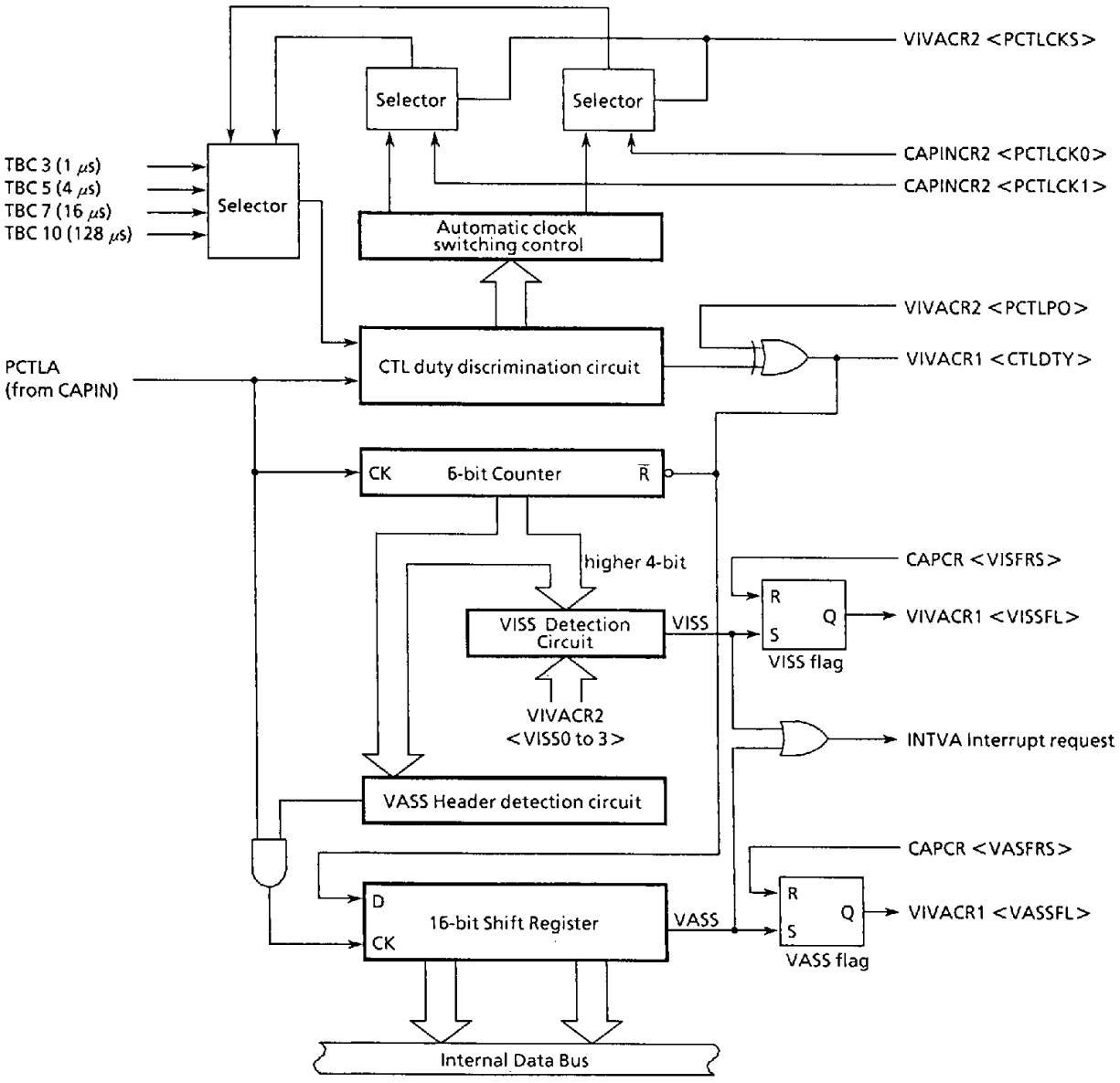


Figure 3.12.1 VISS / VASS detector

3.12.2 Control Registers

VISS / VASS Control Register 1

VIVACR1 (FFF4H)

7	6	5	4	3	2	1	0
"0"	"0"	"0"	"0"		CTLDTY	VISSFL	VASSFL

(Initial value 0000 **00)

CTLDTY	CTL duty discrimination circuit output monitor flag	0 : CTL duty ≧ 50 % (In case of <PCTLPO> = 0) 1 : CTL duty ≦ 50 % (In case of <PCTLPO> = 0)	read only
VISSFL	VISS detect flag	0 : – 1 : VISS detected	
VASSFL	VASS detect flag	0 : – 1 : VASS detected	

Note ; The bit7 to bit4 of the VISS/VASS Control Register 1 (VIVACR1) must be written "0".

VISS / VASS Control Register 2

VIVACR2 (FFF5H)

7	6	5	4	3	2	1	0
PCTLPO	PCTLCKS	$\overline{CDIV}$	$\overline{MSK}$	VISS3	VISS2	VISS1	VISS0

(Initial value 0000 0000)

PCTLPO	Polarity selection of CTL duty discrimination	0 : Positive discrimination (<CTLDTY> is set "1" when CTL duty ≦ 50 %) 1 : Negative discrimination (<CTLDTY> is set "1" when CTL duty ≧ 50 %)	R/W
PCTLCKS	CTL duty measuring clock selection	0 : Selected by <PCTLCK1, PCTLCK0> 1 : Automatic clock selection	
VISS3 to VISS0	VISS detect compare data	4-bit data "0H" to "FH" (This 4-bit data is compared with higher 4-bit data of 6-bit counter.)	

Capture Input Control Register 2

CAPICR2 (FFF6H)

7	6	5	4	3	2	1	0
PCTLCK1	PCTLCK0	PCPR5	PCPR4	PCPR3	PCPR2	PCPR1	PCPR0

(Initial value 0000 0000)

PCTLCK1	CTL duty measuring clock selection (Enable when <PCTLCKS> = 0)	00 : TBC3 01 : TBC5 10 : TBC7 11 : TBC10	R/W
PCTLCK0			

Capture Control Register

CAPCR (FFBEH)

7	6	5	4	3	2	1	0
CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS

(Initial value 0000 0000)

VISFRS	Clearing of VISS flag	0 : – 1 : Clear (One-shot)	R/W
VASFRS	Clearing of VASS flag	0 : – 1 : Clear (One-shot)	

VASS Data Register

VASSDR (FFF8H)

7	6	5	4	3	2	1	0
VASS7	VASS6	VASS5	VASS4	VASS3	VASS2	VASS1	VASS0

(Initial value **** ****)

7	6	5	4	3	2	1	0
VASS15	VASS14	VASS13	VASS12	VASS11	VASS10	VASS9	VASS8

(Initial value **** ****)

VASS7 to VASS0	Lower 8-bit of VASS data	The VASS data can be got by reading of the VASSDR twice. First data is lower 8-bit and second is higher 8-bit.	read only
VASS15 to VASS8	Higher 8-bit of VASS data		

3.12.3 Control of the CTL duty discrimination circuit

(1) Control of CTL duty discrimination

The CTL signal which is amplified by CTL amplifier is inputted, as a PCTLA signal, to VISS/VASS detector (VIVA) via the Capture input control circuit (CAPIN). The CTL duty discrimination circuit judges by threshold; the threshold has half the time of PCTLA signal term. If duty of the PCTLA signal ≧ 50%, the CTL duty discrimination circuit outputs "0". And if its duty ≦ 50 %, it outputs "1". This output can be read as <CTLDTY> of the VISS/VASS control register 1 (VIVACR1). And, the polarity of output can be inverted by using <PCTLPO> of the VISS/VASS control register 2 (VIVACR2).

(2) Control of Clock switching

The Clock source, which is to measure CTL signal term, is selected by software or by hardware. If its clock source is selected by software, it is required to set <PCTLCK0> and <PCTLCK1> in Capture Input Control Register 2 (CAPICR2) to connect adequate TBC while <PCTLCKS> in VIVACR2 is "0". On the other hand, TBC is selected automatically while <PCTLCKS> is "1".
The following table indicates the relation between the term of CTL and its clock source.

Table 3.12.1 Relation between the CTL signal term and its measuring clock source

<PCTLCK1> <PCTLCK0>	Clock source for CTL duty discrimination (at fc = 16 MHz)	Term of CTL signal
00	TBC3 (1 μs)	to 512 μs
01	TBC5 (4 μs)	512 μs to 2048 μs
10	TBC7 (16 μs)	2048 μs to 8192 μs
11	TBC10 (128 μs)	8192 μs to

3.12.4 Control of VISS detection

VISS detection circuit consists of 6-bit up counter counts PCTLA signal, comparator for detecting VISS index code, and R/S flip-flop (VISS flag).
Since CTL duty discriminating output is "L" active reset input for 6-bit counter, 6-bit counter is held on count operation while CTL duty discriminating output is "H" (in case that <PCTLPO> = "0"). The upper 4bits in 6-bit counter are compared with value of VISS detection circuit which is a 4-bit comparator. The data on the comparator is set by <VISS3> to <VISS0> of VISS/VASS Control Register 2 (VIVACR2). VISS signal is outputted when the upper 4bits in 6-bit counter and the data on <VISS3> to <VISS0> are matched; the matching sets the VISS flag and requests INTVA interrupt. The state of VISS flag can be read out by <VISSFL> of VISS/VASS Control Register 1 (VIVACR1), and the VISS flag can be cleared by using <VISFRS> of the Capture control register (CAPCR). Table 3.12.2 shows relation between the value of <VISS3> to <VISS0> and count value of the PCTLA signal.
In order to detect VISS, set VIVACR2 <PCTLPO> to "0" when tape operates forward and set VIVACR2 <PCTLPO> to "1" when it operates reversely.

Table 3.12.2 Relation between the value of <VISS3> to <VISS0> and count value of the PCTLA signal

<VISS3> to <VISS0>				The count value for detecting VISS index code
3	2	1	0	
0	0	0	0	don't use
0	0	0	1	4
0	0	1	0	8
0	0	1	1	12
0	1	0	0	16
0	1	0	1	20
0	1	1	0	24
0	1	1	1	28
1	0	0	0	32
1	0	0	1	36
1	0	1	0	40
1	0	1	1	44
1	1	0	0	48
1	1	0	1	52
1	1	1	0	56
1	1	1	1	60

3.12.5 Control of VASS detection circuit

VASS detector consists of the header detection circuit and address code register (16-bit shift register). The header detection circuit detects the CTL duty discriminating output status that begins with "0" (6-bit counter is reset) before 9bits of continuous "1" (the PCTLA signal is counted by 6-bit counter).

16-bit shift register latches 16bits of CTL duty discriminating output as the address code, which follows "0" after 9bits of "1" in header. When the register finishes latching whole data of 16 bits, R/S flip-flop (VASS flag) is set and INTVA interrupt is requested.

Which interrupt request is generated ; it can be checked by reading <VISSFL> and <VASSFL> of the VISS/VASS control register 1 (VIVACR1) in INTVA interrupt processing routine. VASS flag can be reset to "0" by using <VASFRS> of the Capture control register (CAPCR).

VASS address code generates INTVA interrupt 4 times by one set because address code has 4 headers. But the 4th code data becomes dummy. And, when the INTVA interrupt is generated, it is required to read address code before the next address code is started to latch. The 16-bit address code can be got by reading VASS data register (VASSDR) twice; the first read data is lower 8-bit (<VASS7> to <VASS0>) of the address code and the second read data is higher 8-bit (<VASS15> to <VASS8>). In addition, if data is written to VASSDR (dummy write), the VASSDR gets ready for reading lower 8-bit.

In order to detect VASS, set VIVACR2 <PCTLPO> to "0" when the tape operates forward and set VIVACR2<PCTLPO> to "1" when the tape operates reversely. Notice that the LSB and MSB of address code are reversed each other in case the tape operates reversely.

3.13 Head Amp / Color Rotary Control Circuit

The TMP90CR74A contains the output circuit to control Head Amp / Color Rotary. HA output / CR output can control shifting drum-head amplifier by logical combination, consists of TPG03 (from TPG0), TPG05 (from TPG0), and Head Amp control register (HACR).

3.13.1 Configuration

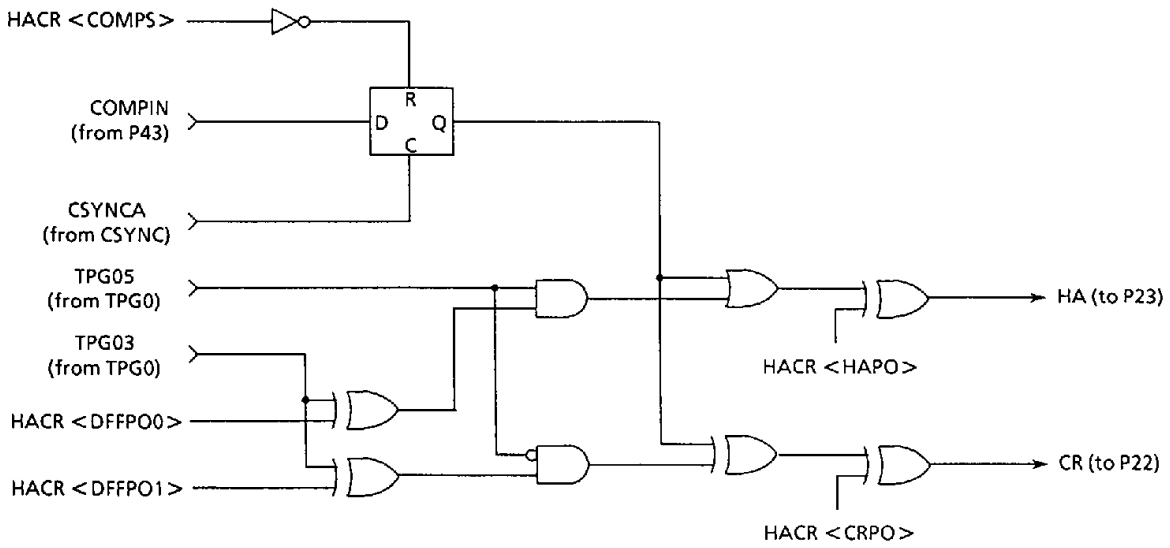


Figure 3.13.1 Head Amp / Color Rotary control circuit

3.13.2 Control Registers

Head Amp control register

HACR (F794H)

7	6	5	4	3	2	1	0
CRMOD	"0"	VTPE34	DFFPO1	DFFPO0	COMPS	CRPO	HAPO

(Reset Value 0000 0000)

CRMOD	Selection for P22 / P23 / P43 mode	0 : I/O port 1 : CR (P22) / HA (P23) / COMPIN (P43)	R/W
DFFPO1	Polarity shifting for TPG03 input	0 : Positive polarity 1 : Negative polarity	
DFFPO0	Polarity shifting for TPG03 input	0 : Positive polarity 1 : Negative polarity	
COMPS	Enable / disable for COMPIN (P43) input	0 : Disable 1 : Enable	
CRPO	Polarity shifting for CR output	0 : Positive polarity 1 : Negative polarity	
HAPO	Polarity shifting for HA output	0 : Positive polarity 1 : Negative polarity	

Note) Always writing "0" in bit 6 of Head Amp control register (HACR)

3.13.3 Utilizing Head Amp / Color Rotary

(1) Logic architecture and operation mode

Controlling HA (Head Amp) / CR (Color Rotary) output is executed by TPG03, TPG05 and HACR, as described below.

$$HA = <HAPO> \oplus [(CMPIN \cdot <COMPS>) + (TPG05 \cdot (TPG03 \oplus <DFFPO0>))]$$
$$CR = <CRPO> \oplus [(CMPIN \cdot <COMPS>) \oplus (\overline{TPG05} \cdot (TPG03 \oplus <DFFPO1>))]$$

Usually, while device operates as HA shifting or CR output HA output and output are classified to following 3 operation mode.

Table 3.13.1 HA / CR output operate mode

Mode	<COMPS>	TPG05	HA output	CR output
mode 1	0	0	<HAPO>	<CRPO> ⊕ (TPG03 ⊕ <DFFPO1>)
mode 2	0	1	<HAPO> ⊕ (TPG03 ⊕ <DFFPO0>)	<CRPO>
mode 3	1	0	<HAPO> ⊕ COMPIN	<CRPO> ⊕ COMPIN ⊕ (TPG03 ⊕ <DFFPO1>)

In these cases, TPG03 is utilized as DFF. The polarity is shifted on <DFFPO0>, <DFFPO1>. TPG05 shift the mode among mode 1 thru 3. <COMPS> controls the input signal CMPIN (P43) input, which is to compare the frequency modulation signal for SP / EP head.

(2) Example

The following timing chart indicates the HA, CR output, assuming <HAPO> = <CRPO> is SP and <DFFPO0> = <DFFPO1> = 1, under the circuit described below.

Assuming that CR output is CH1 for high level and CH2 for low level.

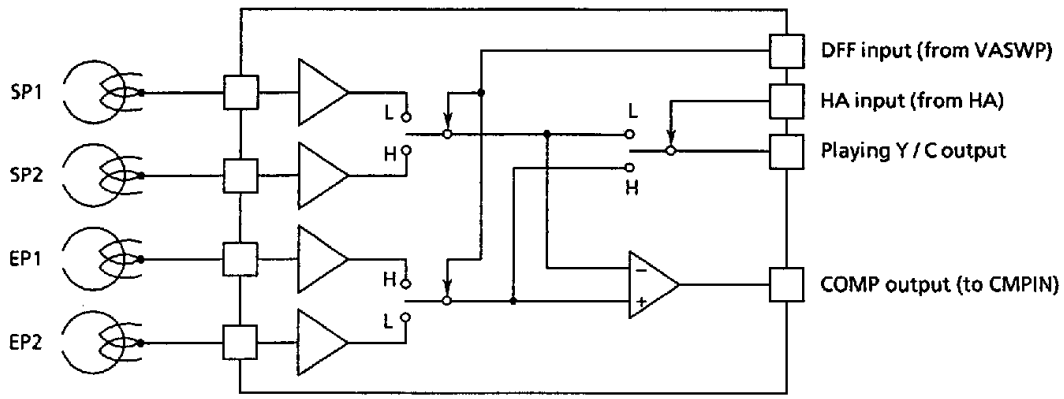


Figure 3.13.2 Example for the interface with Rec / Pre amplifier

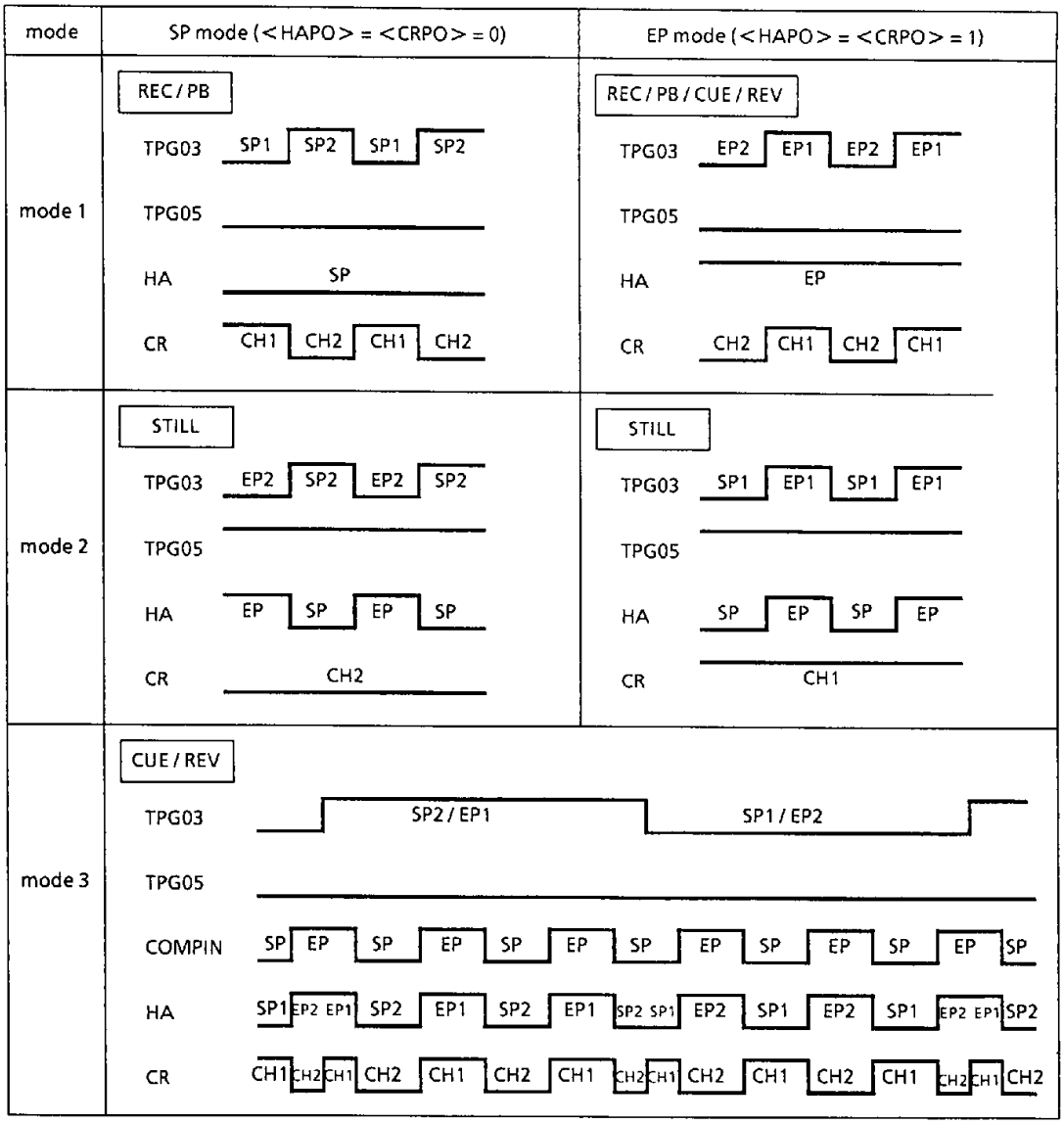


Figure 3.13.3 HA / CR output sequence

The basic operation, such as REC / PB, STILL, CUE / REV, can be executed by mode setting, as described above. The SLOW operation can be set by cycling between mode 1 and mode 2 (shifted on TPG05).

3.13.4 VASWP output control

The output TPG03 of TPG0 can be used for drum-head shifting signal (DFF) ; it can be obtained from VASWP terminal.

The following diagram shows the circuit for VASWP.

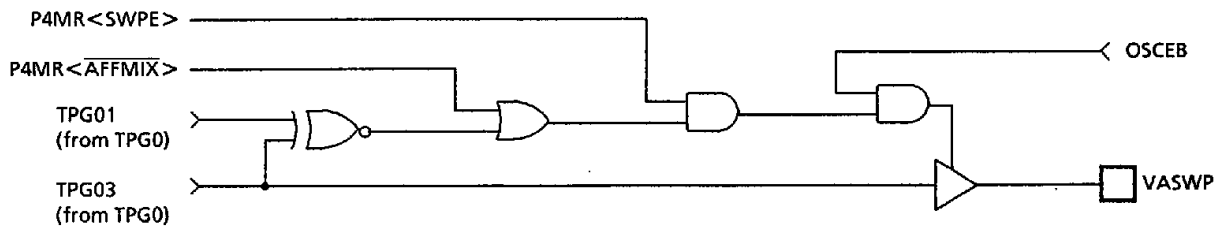


Figure 3.13.4 Circuit for VASWP output

① Control register

VASWP output can be controlled by P4 mode register (P4MR).

P4 mode register

P4MR (F785H)

7	6	5	4	3	2	1	0
AFFMIX	SCLK1E	RXD1E	SWPE	BLKE	TXD1E	RGBE	DOTXE

(Reset Value 0000 0000)

AFFMIX	Control AFF signal mix	0 : Mix DFF with AFF 1 : Output only DFF	R/W
SWPE	VASWP output enable	0 : Disable 1 : Enable	

② Utilizing VASWP output

Use DFF for TPG03 and AFF for TPG01.

P4 mode register (P4MR) <AFFMIX> can select the output: DFF only or mixed DFF with AFF: If AFF is mixed, the VASWP becomes 3-rate output. The VASWP output can be controlled whether to enable or to disable.

The following diagram indicates the timing chart for VASWP output.

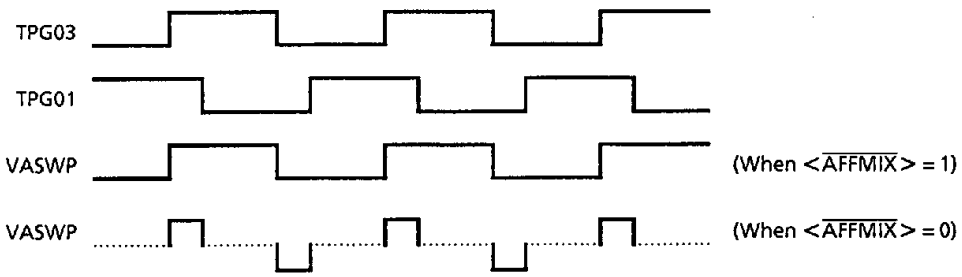


Figure 3.13.5 Timing chart for VASWP output

3.14 SYNC SIGNAL SEPARATOR (CSYNC)

The Sync Signal Separator separates the Vertical Synchronizing Signal (V.SYNC) and Horizontal Synchronizing Signal (H.SYNC) from composite synchronizing signal (C.SYNC signal).

3.14.1 Configuration

The Sync Signal Separator consists of H/V Separator, Mute Detector and H.Pulse Generator.
A configuration of the Sync Signal Separator is shown in Figure 3.14.1.

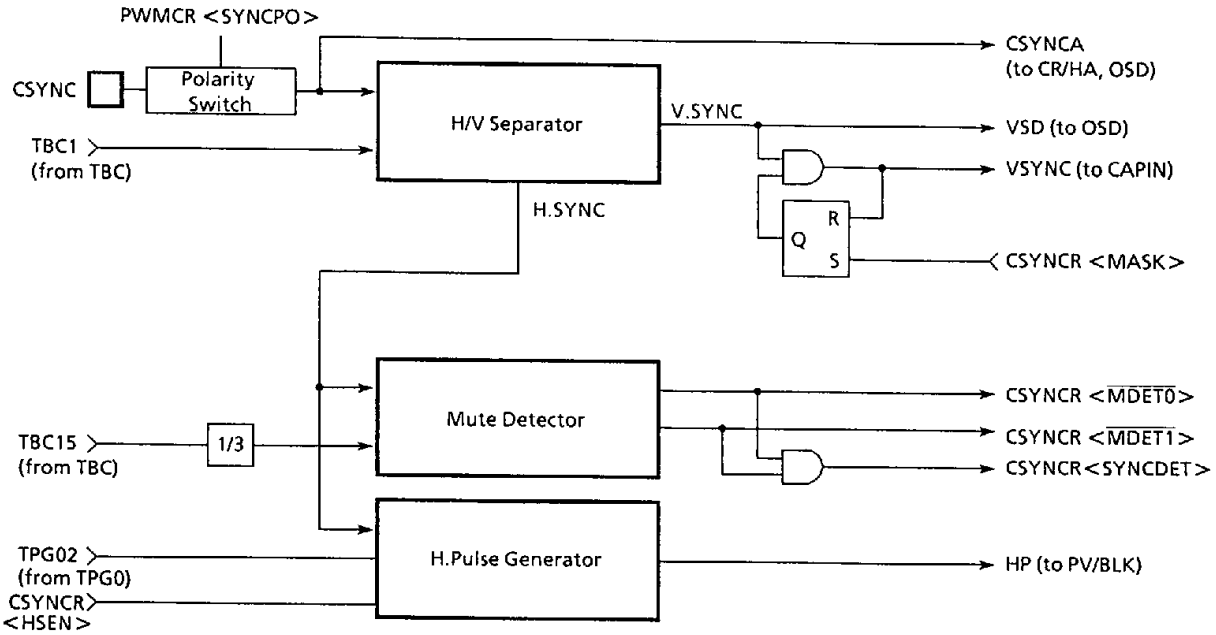


Figure 3.14.1 Configuration of Sync Signal Separator

(1) H/V Separator

The H/V separator separates H.SYNC and V.SYNC signals from the C.SYNC inputted from CSYNC pin. A separated V.SYNC signal is transferred to Capture 0 (CAP0) via the Capture input control circuit (CAPIN). And it is used for reference signal in the servo processing routine. In addition, V.SYNC signal is transferred to On Screen Display circuit (OSD) and it is used for a synchronizing signal in display control circuit.

A separated H.SYNC signal is inputted to the Mute Detector and H.Pulse generator.

(2) Mute Detector

The mute detector counts H.SYNC signal separated from C.SYNC signal and judges it a normal C.SYNC signal or mute state (no signal).

The mute detector's output can be read out from <$\overline{\text{MDET1}}$>, <$\overline{\text{MDET0}}$> and <SYNCDET> of the CSYNC control register (CSYNCR).

When normal C.SYNC signal is inputted, <SYNCDET> is "1". And when mute state is detected, "0" is read out from <SYNCDET>, further, information about mute state can be got from mute detection flags (<$\overline{\text{MDET1}}$>, <$\overline{\text{MDET0}}$>).

(3) H.Pulse Generator

The H.Pulse generator generates serrated-pulse (HP signal), synchronizing with H.SYNC signal from C.SYNC, in pseudo-V.SYNC signal.

The HP signal is transferred to the Pseudo-sync signal output circuit (PV/BLK), and it is superimposed to the pseudo-V.SYNC signal as serrated-pulse.

(Refer to 3.15 Pseudo-sync signal output circuit.)

3.14.2 Control Registers

CSYNC Control Register

CSYNCR (FFFDH)

7	6	5	4	3	2	1	0
AVDP0	AHDP0	$\overline{\text{MDET1}}$	$\overline{\text{MDET0}}$	SYNC DET	HSEN	MASK	

(Initial value 0010 000*)

$\overline{\text{MDET1}}$	Mute detection flag	0 : Mute detect (noisy composite sync signal) 1 : Normal	read only
$\overline{\text{MDET0}}$	Mute detection flag	0 : Mute detect (no signal) 1 : Normal	
SYNCDET	Sync signal detection flag	0 : Mute detect 1 : Normal	
HSEN	H.pulse (HP) control	0 : Non-synchronize HP with C.SYNC 1 : Synchronize HP with C.SYNC	R/W
MASK	V.SYNC masking control	0 : – 1 : Release masking (one-shot)	

PWM control register

PWMCR (F793H)

7	6	5	4	3	2	1	0
	PWM 01M	CFRTRGS	SYNCPO	PWMSEL	PWMPO2	PWMPO1	PWMPO0

(Initial value *000 0000)

SYNCPO	Switching polarity of C.SYNC signal	0 : Positive 1 : Invert	R/W

3.14.3 H/V Separator

The H/V Separator Separates the Vertical Synchronizing Signal (V.SYNC) and Horizontal Synchronizing Signal (H.SYNC) from Composite Synchronizing Signal inputted from CSYNC pin.

The H/V Separator consists of 7-bit up/down counter and pattern detector (compare / match circuit). Configuration of the H/V Separator is shown in Figure 3.14.2.

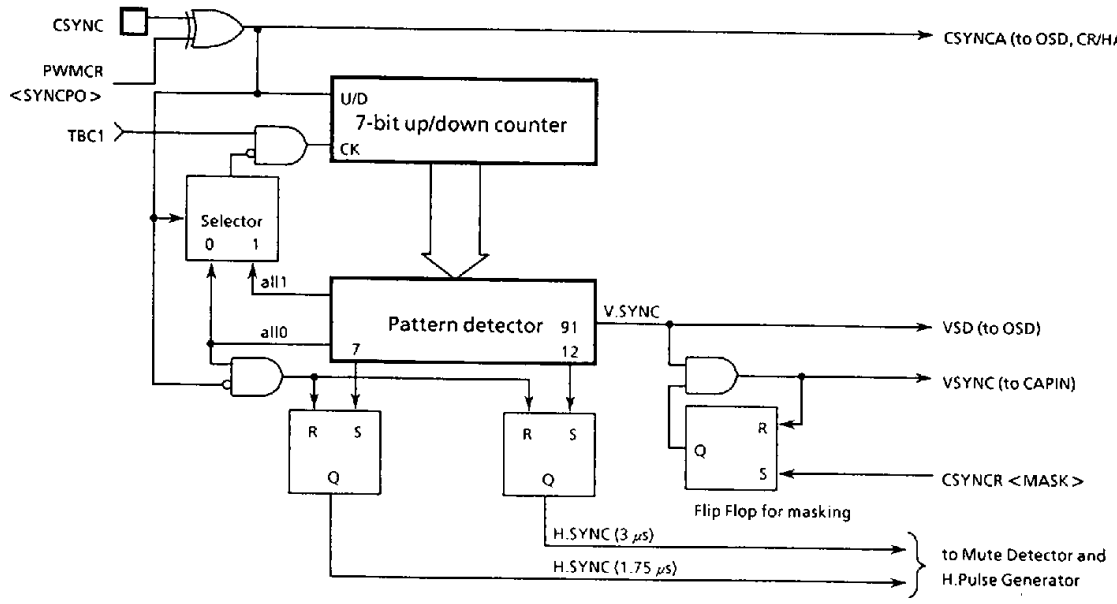


Figure 3.14.2 H/V Separator

7-bit up/down counter counts TBC1 (22/fc) output from the Time Base Counter. And its direction for counting is controlled by input polarity of CSYNC pin; CSYNCA = "1" is for up count and CSYNCA = "0" is for down count. The input polarity of CSYNC pin (CSYNCA signal) is selected by setting <SYNCPO> in PWM control register (PWMCR) and it controls the direction for counting 7-bit counter. In case that CSYNCA is "1", counter stops when counter output becomes all "1". And in case that CSYNCA is "0", counter stops when counter output becomes all "0".

(1) V.SYNC separation

If pattern detector (compare/match circuit) detects "91 (5BH)" (TBC1 term : 250 [ns] at fc = 16 [MHz]. Therefore, threshold rate is 250 [ns] × 91 = 22.75 [μs]), it outputs the V.SYNC signal. V.SYNC enables VSD signal (to OSD) and VSYNC signal (to CAP0), and it resets flip-flop for masking. Flip-flop for masking are reset once, the following V.SYNC signals are not accepted until masking is released. Setting flip-flop (to release masking) is executed on <MASK> of CSYNC control register (CSYNCR). Timing chart of V.SYNC separation is show in Figure 3.14.3.

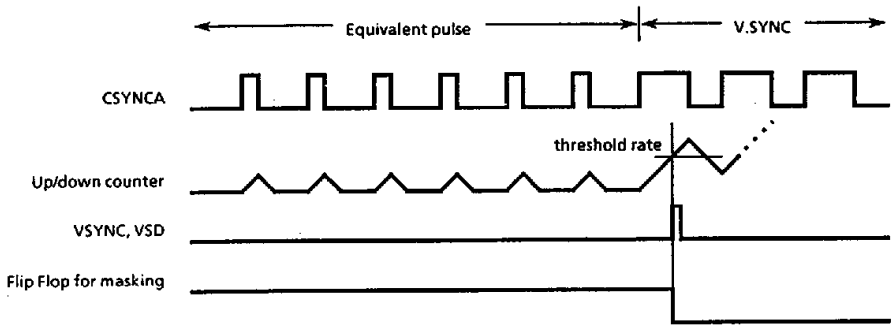


Figure 3.14.3 Timing Chart for V.SYNC separation

(2) H.SYNC separation

If pattern detector detects "7 (7H)" or "12 (CH)" (TBC1 term : 250 [ns] at fc = 16 [MHz]. Therefore, threshold rate is 250 [ns] × 7 = 1.75 [μs] or 250 [ns] × 12 = 3.0 [μs]), it outputs the H.SYNC signal (1.75 μs / 3.0 μs). In case that CSYNCA signal is "0", H.SYNC signal is reset when 7-bit counter becomes all "0". H.SYNC (1.75 μs) signal and H.SYNC (3.0 μs) signal, which are separated by H/V Separator, is transferred to the Mute Detector and H.Pulse generator.

3.14.4 Mute Detector

The mute detector detects mute state of C.SYNC signal by counting H.SYNC signal. Configuration of the Mute Detector is shown in Figure 3.14.4.

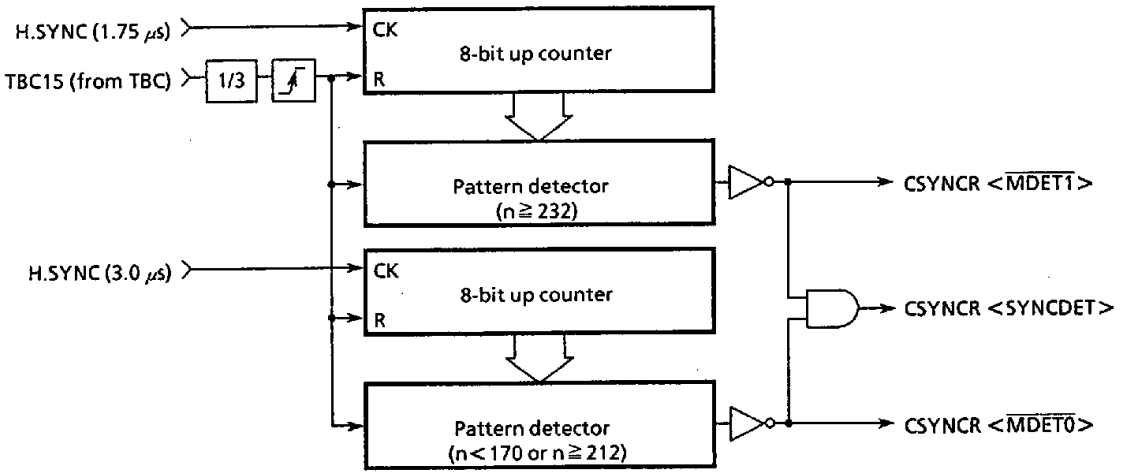


Figure 3.14.4 Mute Detector

The mute detector consists of 2 types of pattern detector (compare/match) with 8-bit up counter; one is for H.SYNC (1.75 μs) signal, the other one is for H.SYNC (3.0 μs) respectively. It performs a detection at every TBC15 / 3 (12.3 [ms] at fc = 16 [MHz]).

(1) Mute Detection Flag <$\overline{\text{MDET1}}$>

The 8-bit up counter counts H.SYNC (1.75 μs) signal. If count value exceeds 232 during a detection period (12.3 ms), <$\overline{\text{MDET1}}$> will be reset to "0" as there are noise in the C.SYNC signal. <$\overline{\text{MDET1}}$> is set to "1" by reset operation, and it keeps "1" as far as input is normal signal. <$\overline{\text{MDET1}}$> is located on bit 5 in the CSYNC control register (CSYNCR).

(2) Mute Detection Flag <$\overline{\text{MDET0}}$>

The 8-bit up counter counts H.SYNC (3.0 μs) signal. When count value is more than 170 and less than 212 during a detection period, <MDET0> keeps "1" as there is normal C.SYNC signal. But if count value is less than 170 or more than 212, <$\overline{\text{MDET0}}$> will be reset to "0" as there is uncertain signal. <$\overline{\text{MDET0}}$> is reset to "0" by reset operation, then it will be set to "1" by inputting normal signal. <$\overline{\text{MDET0}}$> is located on bit 4 in the CSYNC control register (CSYNCR).

(3) Sync signal Detection Flag <SYNCDET>

Since <SYNCDET> is logical-AND between <$\overline{\text{MDET1}}$> and <$\overline{\text{MDET0}}$>, data "1" is read out from <SYNCDET> as far as input is normal signal. <SYNCDET> is reset to "0" by reset operation, then it will be set to "1" by inputting normal C.SYNC signal. <SYNCDET> is located on bit 3 in the CSYNC control register (CSYNCR).

3.14.5 H.PULSE Generator

H.SYNC Generator generates serrated pulse in V.SYNC signal. This generated pulse (HP signal) is transferred to Pseudo-sync signal output circuit (PV/BLK), and it can be mixed to pseudo-V.SYNC signal. Configuration of the H.Pulse generator is shown in Figure 3.14.5.

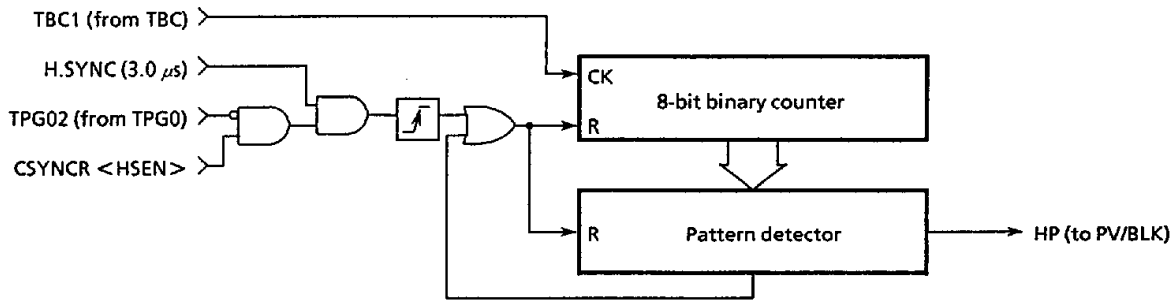


Figure 3.14.5 H.Pulse Generator

H.Pulse Generator generates serrated pulse (HP signal) to mix with pseudo-V.SYNC. The timing to mix pseudo-V.SYNC with HP signal is controlled by TPG02 from the Timing pulse generator 0 (TPG0) (Refer to section 3.15 Pseudo-sync signal output circuit). By setting <HSEN> in CSYNC control register (CSYNCR) to "1", HP signal can be synchronized with the H.SYNC (3.0 μs) signal, outputted from H/V Separator, during TPG02 is "L". In case that <HSEN> is "0", HP signal is not synchronized with C.SYNC signal input. Wave form of the HP signal output is shown in Figure 3.14.6.

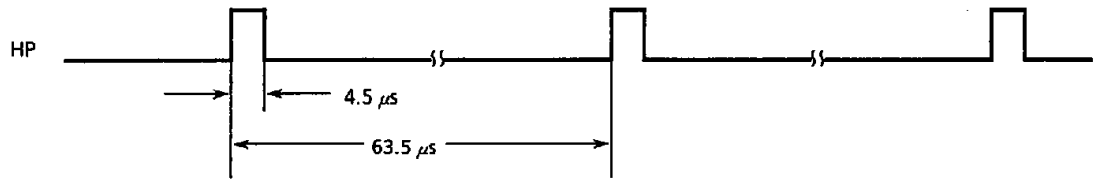


Figure 3.14.6 Wave form of HP signal output

3.15 Pseudo-sync Signal Output Circuit (PV/BLK)

The TMP90CR74 has a function to output a pseudo-sync signal (PV) in place of the playback sync signal during special effect reproduction. The PV output is controlled by the timing pulse generator 0 (TPG0)'s TPG02 and TPG04 outputs and the PV control register (PVCR).

3.15.1 Circuit Configuration

The pseudo-sync signal output circuit consists of a sync signal mixing circuit, a blanking signal mixing circuit, and a 4-level output circuit. The sync signal mixing circuit is used to superimpose the serrated pulse (HP) that is generated by the H pulse generator of the sync signal separation circuit (CSYNC) on a pseudo-V.SYNC signal. The blanking signal mixing circuit is used to synthesize the sync signal mixing circuit output and on-screen display output blanking signal (BLK).

Figure 3.15.1 shows a configuration of the pseudo-sync signal output circuit.

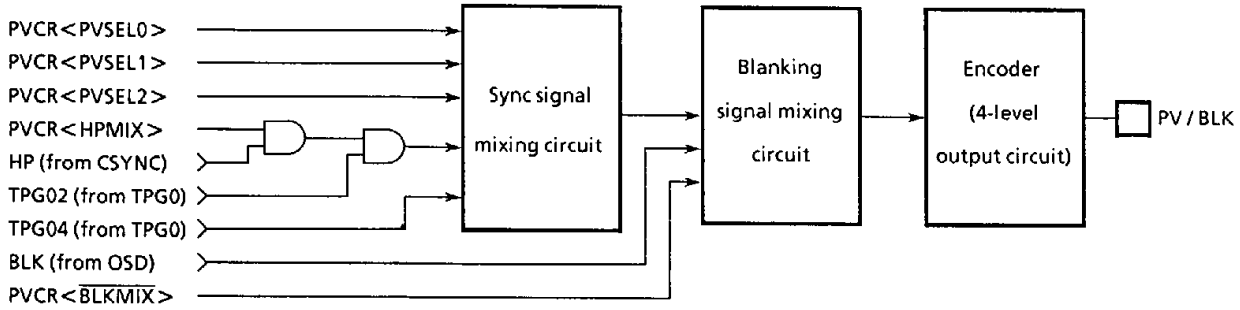


Figure 3.15.1 Configuration of the pseudo-sync signal output circuit

3.15.2 Control Register

PV control register

PVCR (F799H)

7	6	5	4	3	2	1	0
XOON	S/N	"0"	$\overline{\text{BLKMIX}}$	HPMIX	PVSEL2	PVSEL1	PVSEL0

(Initial value 0000 0000)

$\overline{\text{BLKMIX}}$	Mix BLK signal (from OSD).	0 : Mixed 1 : Not mixed	R/W
HPMIX	Mix HP signal (from CSYNC).	0 : Mixed 1 : Not mixed	
PVSEL2 to PVSEL0	Select PV/BLK output format.	Output format is selected with 0(H) to 7(H).	

Always write "0" to bit 5 in PV control register (PVCR)

3.15.3 Control of Pseudo-sync Signal Output

Output of the pseudo-sync signal (PV) is controlled by TPG02 and TPG04 outputs of the timing pulse generator 0 (TPG0) and the PV control register (PVCR).

The vertical sync signal (V.SYNC) is patterned by the TPG0 which is output from TPG04. The TPG02 output is used to set a period at which time the serration (serrated pulse) of V.SYNC is inserted. The serration (HP signal) is generated by the H pulse generator of the sync signal separation circuit (CSYNC). The HP signal is inserted into V.SYNC by setting the PVCR register PHMIX bit to 1.

The pseudo-sync signal has six output formats which can be selected by the PVCR register's PVSEL2-0 bits. Figure 3.15.2 shows the output formats of the pseudo-sync signal.

3.15.4 On-screen Display Output Blanking Signal (BLK)

When using the PV/BLK pin for pseudo-sync signal output, the above six types of output formats are output at three voltage levels. However, with the PVCR register BLKMIX bit cleared to 0, they can be output at four voltage levels by superimposing the blanking signal (BLK) of the on-screen display (OSD) output on the pseudo-sync signal (PV). In this case, the PV and BLK signals must be separated external to the pin. Since the BLK signal also is multiplexed on the P42 (BLK/TxD1) pin, the P42 pin can be used as a general-purpose I/O port (P42) or serial transmit pin (TxD1) by setting the PV/BLK pin for 4-voltage level output. The P42 (BLK/TxD1) pin is a normal three-value output.

The BLKMIX bit is reset to 0 by the device's initialize operation.

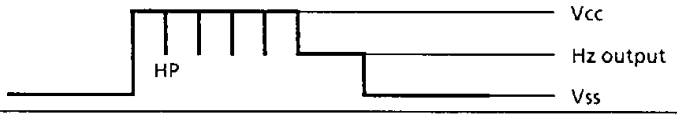
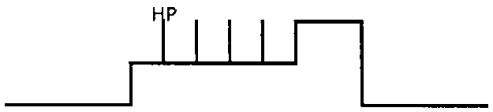
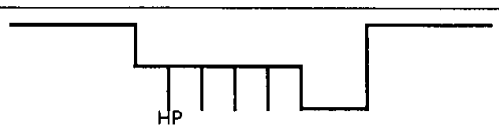
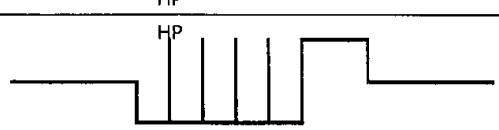
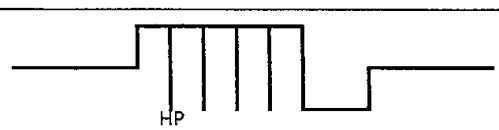
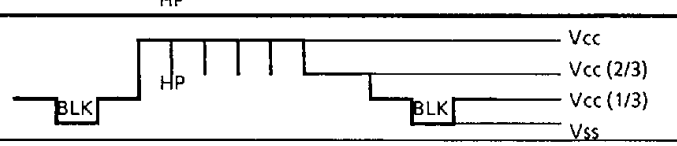
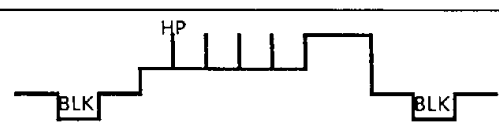
<$\overline{BLKMIX}$>	<PVSEL 2 to 0>			TPG02 / TPG04 (<PHMIX> = 1)
	2	1	0	
1	0	0	0	
	0	0	1	
	0	1	0	
	0	1	1	
	1	*	0	
	1	*	1	
0	0	0	0	
	0	0	1	

Fig 3.15.2 Pseudo-Vsync output format

3.16 ON-SCREEN DISPLAY CIRCUIT (OSD)

TMP90CR74A has On Screen Display (OSD) circuit for displaying characters and symbols on TV screen on chip. The character and symbol font is in Character Font ROM, put characters or symbols in display RAM for display message on TV screen. This function can be used to display VCR recording menu and message.

3.16.1 OSD Functional Outline

TMP90CR74A OSD functional outline are shown in Table 3.16.1.

Broadcasting System			NTSC · PAL · M-PAL · N-PAL · 60PAL · 4.43NTSC
Screen Configuration	Horizontal		24 characters
	Vertical		10 lines (line space 0, 1, 2, 4 dot selectable)
	Number of Character		Max. 240 characters
	Font	Horizontal	12 dots
		Vertical	18 dots
Character	Kind of character		Max. 256 (4-type blank code included)
	Size	Unit	Size for 1st line and other lines (2nd to 10th) can be set independently
		Type	16 (Horizontal x1, x2, x3, x4, Vertical x1, x2, x3, x4)
	Display Style	Unit	Style for 1st, Mth thru Nth (set by command) and other lines can be set independently
		Type	Fringing (4 channels), Non-Fringing (3 channels) : black fringing only
Fringing		Horizontal	1TC (1 dot)
		Vertical	1HD (1 dot)
Smoothing			Smoothing available in x2 or x4 mode of character size
Display Starting position		Horizontal	16 position (unit : 4TC)
		Vertical	16 position (unit : 4HD)
Blinking		Unit	each character
		Type	6 (Blinking frequencies : 2) × (duty : 3)
		Style	Normal, Reverse, Flip
Color		Unit	Screen (Color for character, character background and background can be set independently)
		Type	Hue (Tint) : 8, Value (Luminance) : 5, non-coloring

TC: Dot clock, HD: Horizontal Sync signal

Table 3.16.1 OSD function

3.16.2 Configuration

On Screen Display (OSD) cirucuit has three main control registers (OSDCR, OSDADR, OSDDBR), eight display mode control registers (OSDMR0 to 7), display control RAM, character ROM, character generator, clock generator, Sync. generator, video encoder, video signal output amps.

OSD circuit composition are shown in Fig 3.16.1.

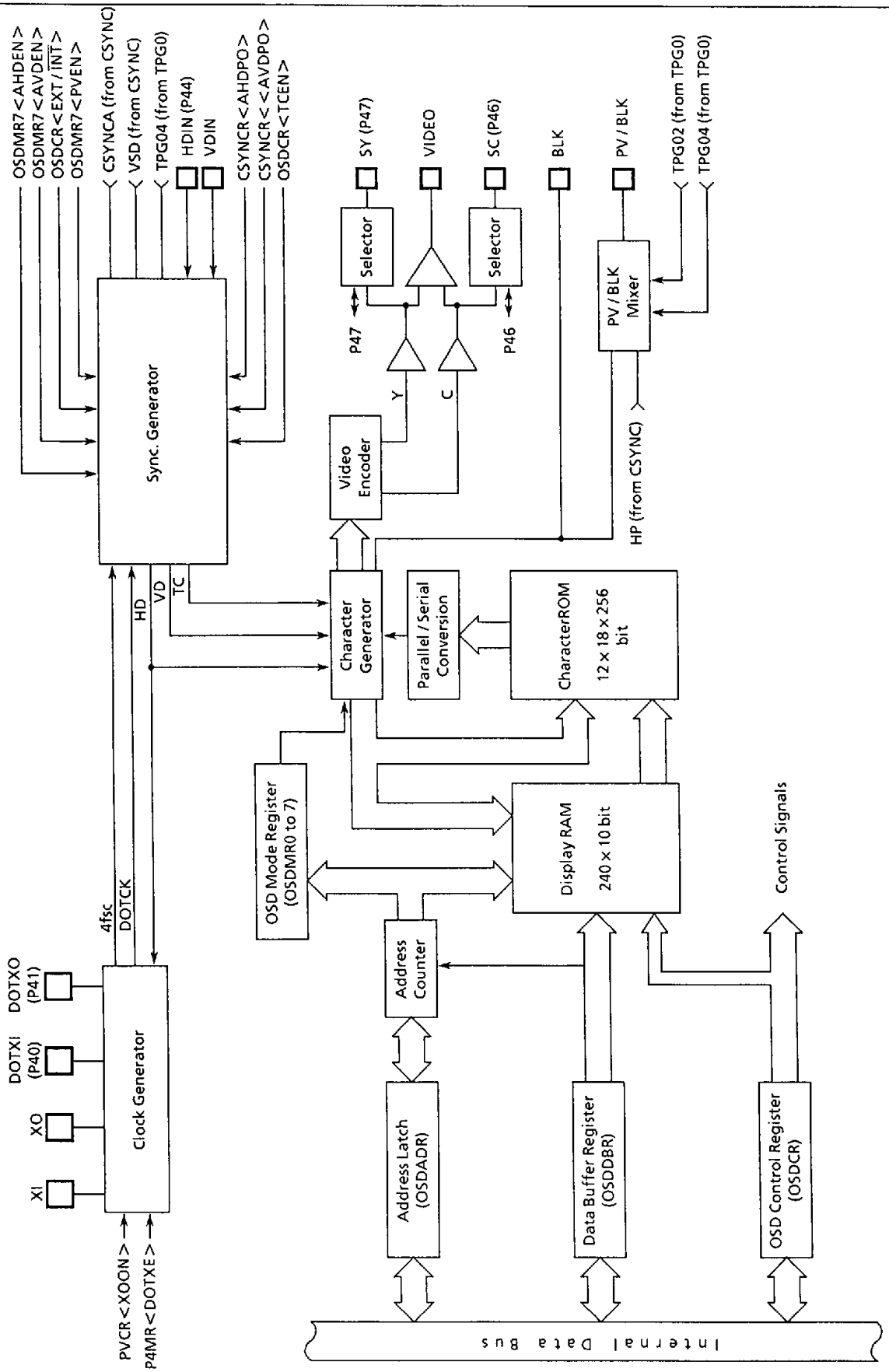


Fig 3.16.1 On Screen Display Circuit Block Diagram

3.16.3 Memory Configuration

On screen display (OSD) circuit uses following four (4) kinds of memories,

① Three (3) Main Control Registers : OSD Control Register (OSDCR), Display RAM Address Register (OSDADR) display, Data Buffer Register (OSDDBR)
② OSD Mode Register (OSDMR0) to (OSDMR7)
③ Display RAM (240 × 10-bit)
④ Character ROM for Character Font (18 × 12 × 256-bit)

(1) Main Control Registers

Main Control Registers are OSDCR (address FFCEH), OSDADR (address FFCFH) and OSDDBR (address FFD0H).

The main control registers can be accessed by CPU directly. Although data can not be set to Display RAM and OSD Mode Registers (OSDMRn) directly, data can be set through main control register (OSDADR, OSDDBR) by CPU indirectly. Data written in Display RAM and OSDMRn can not be read out.

OSD Control Register

OSDCR (FFCEH)

7	6	5	4	3	2	1	0
CMD1	CMD0	TCEN	DISPON	EXT/$\overline{INT}$	4/3	50/$\overline{60}$	P/$\overline{N}$

(Reset Value 0000 0000)

CMD1 CMD0	Character display style selection (Blinking mode)	Actual display style is related with <MOD> bit in OSDMR4 register. *	R/W
TCEN	Dot clock (TC) enable	0 : Disable 1 : Enable	
DISPON	Display enable	0 : Disable 1 : Enable	
EXT/$\overline{INT}$	Display synchronization	0 : Internal mode (full page mode) 1 : External mode (Superimpose mode)	
4/$\overline{3}$	Selection of color sub-carrier (fsc) for full-page mode	0 : 3.58 MHz 1 : 4.43 MHz	
50/$\overline{60}$	Selection of V-sync frequency (fv) for full-page mode	0 : 60 Hz 1 : 50 Hz	
P/$\overline{N}$	PAL / NTSC	0 : NTSC 1 : PAL	

* See chapter 3.16.10 that indicates "Blinking"

Display RAM Address Setup Register

OSDADR (FFCFH)

7	6	5	4	3	2	1	0
OSDA7	OSDA6	OSDA5	OSDA4	OSDA3	OSDA2	OSDA1	OSDA0

(Reset Value 0000 0000)

OSDA7 to OSDA0	Address data for Display RAM (00H to EFH) or OSD (F0H to F7H) mode register	R/W

Display RAM Data Buffer Register

OSDDBR (FFD0H)

7	6	5	4	3	2	1	0
OSDD7	OSDD6	OSDD5	OSDD4	OSDD3	OSDD2	OSDD1	OSDD0

(Reset Value 0000 0000)

OSDD7 to OSDD0	Data buffer for Display RAM or OSD mode register	R/W

(2) OSD MODE Registers

OSD Mode Control Registers are eight (8) bytes registers which can be accessed indirectly through Main Control Registers OSDADR and OSDDBR. These eight (8) registers (OSDMR0) to (OSDMR7) are located at indirect address 0F0H to 0F7H.

OSD Mode Register 0

OSDMR0 (00F0H)

7	6	5	4	3	2	1	0
POSV3	POSV2	POSV1	POSV0	POSH3	POSH2	POSH1	POSH0

(Reset Value 0000 0000)

POSV3 to POSV0	Vertical start position	Select 16 starting position (x 4HD)	write only
POSH3 to POSH0	Horizontal start position	Select 16 starting position (x 4TC)	

OSD Mode Register 1

OSDMR1 (00F1H)

7	6	5	4	3	2	1	0
FSV1	FSV0	FSH1	FSH0	CSV1	CSV0	CSH1	CSH0

(Reset Value 0000 0000)

FSV1 FSV0	Character size of 1st line	Vertical size (x 1, 2, 3, 4)	write only
FSH1 FSH0		Horizontal size (x 1, 2, 3, 4)	
CSV1 CSV0	Character size of 2nd to 10th line	Vertical size (x 1, 2, 3, 4)	
CSH1 CSH0		Horizontal size (x 1, 2, 3, 4)	

OSD Mode Register 2

OSDMR2 (00F2H)

7	6	5	4	3	2	1	0
MSL3	MSL2	MSL1	MSL0	NSL3	NSL2	NSL1	NSL0

(Reset Value 0000 0000)

MSL3 to MSL0	Mth line	$M = \sum_{n=0}^{3} 2^n \cdot MSLn + 1$ (th Line)	write only
NSL3 to NSL0	Nth line	$N = \sum_{n=0}^{3} 2^n \cdot NSLn + 1$ (th Line)	

OSD Mode Register 3

OSDMR3 (00F3H)

7	6	5	4	3	2	1	0
SPACE1	SPACE0	GLD1	GLD0	NLD1	NLD0	FLD1	FLD0

(Reset Value 0000 0000)

SPACE1 SPACE0	Line space	00 : 0HD 10 : 2HD 01 : 1HD 11 : 4HD	write only
GLD0	Fringing for general line (Except 1st and Mth to Nth line)	0 : Fringing off 1 : Fringing on	
GLD1	Character background for general line (Except 1st and Mth to Nth line)	0 : Character background off 1 : Character background on	
NLD0	Fringing for Mth to Nth line	0 : Fringing off 1 : Fringing on	
NLD1	Character background for Mth to Nth line	0 : Character background off 1 : Character background on	
FLD0	Fringing for 1st line	0 : Fringing off 1 : Fringing on	
FLD1	Character background for 1st line	0 : Character background off 1 : Character background on	

OSD Mode Register 4

OSDMR4 (00F4H)

7	6	5	4	3	2	1	0
CB/$\overline{CF}$	FCPH2	FDPH2	FEPH2	MOD	BLINK2	BLINK1	BLINK0

(Reset Value 0000 0000)

CB/$\overline{CF}$	Area selection for color changing by Blank code	0 : Character font 1 : Character background	write only
FCPH2	Character or its background coloring after display position of Blank code (FCH)	PH2 of hue setting changed by Blank code (FCH)	
FDPH2	Character or its background coloring after display position of Blank code (FDH)	PH2 of hue setting changed by Blank code (FDH)	
FEPH2	Character or its background coloring after display position of Blank code (FEH)	PH2 of hue setting changed by Blank code (FEH)	
MOD	Blinking mode	Displaying style is determined with <CMD1, 0> bit in OSDCR register.	
BLINK2	Blinking time	0 : 2^5/fv [s] 1 : 2^6/fv [s] (fv : Frequency of V-sync)	
BLINK1	Blinking duty	00 : Blinking off 01 : 1/4 duty 10 : 2/4 duty 11 : 3/4 duty	
BLINK0			

OSD Mode Register 5

OSDMR5 (00F5H)

7	6	5	4	3	2	1	0
BGOFF	BGPH2	BGPH1	BGPH0	CBOFF	CBPH2	CBPH1	CBPH0

(Reset Value 0000 0000)

BGOFF	Coloring of background screen	0 : ON 1 : OFF	write only
BGPH2 to BGPH0	Hue of background screen	8 kinds of color (hue) at every 45 deg. against color-burst (0 to 7H)	
CBOFF	Coloring of character background	0 : ON 1 : OFF	
CBPH2 to CBPH0	Hue of character background	8 kinds of color (hue) at every 45 deg. against color-burst (0 to 7H)	

OSD Mode Register 6

OSDMR6 (00F6H)

7	6	5	4	3	2	1	0
"0"	YL2	YL1	YL0	CFOFF	CFPH2	CFPH1	CFPH0

(Reset Value 0000 0000)

YL2 to YL0	Luminance (Y) level	Selecting from 5 to 100 IRE	write only
CFOFF	Coloring of character font	0 : ON 1 : OFF	
CFPH2 to CFPH0	Hue of character	8 kinds of color (Hue) at every 45 deg. against color-burst (0 to 7H)	

Note) Write "0" in bit 7 of OSDMR6

OSD Mode Register 7

OSDMR7 (00F7H)

7	6	5	4	3	2	1	0
SPON	SMOOTH	EQON	NONINT	RATIOHV	PVEN	ADVEN	AHDEN

(Reset Value 0000 0000)

SPON	Area selection of line space (Line space between Mth and Nth : Character background)	0 : Background of screen (Note 1) 1 : Character background	write only
SMOOTH	Smoothing	0 : Disable 1 : Enable	
EQON	Equalizing pulse in non-interlace mode	0 : OFF 1 : ON	
NONINT	Interlace/Non-interlace display	0 : Interlace 1 : Non-interlace (Note 2)	
RATIOHV	Setting frquency ratio between VD and HD in full page mode	The frequency ratio between HD and VD results from OSDCR <50/60>, <NONINT> and <RATIOHV>.	
PVEN	VD input switching	0 : External VDIN or VSD from Csync 1 : TPG04	
ADVEN	External VDIN	0 : Disable 1 : Enable	
AHDEN	External HDIN (P44)	0 : Disable 1 : Enable	

(Note 1) Line space between Mth and Nth line set by OSDMR2 is fixed to character background, no matter what the <SPON> is.

(Note 2) Although the OSD doesn't care an even/odd field, the non-interlace display doesn't have vertical jitter in full-page mode.

PV / PH Control Register

PVCR (F799H)

7	6	5	4	3	2	1	0
XOON	S/N	"0"	BLKMIX	PHMIX	PVSEL2	PVSEL1	PVSEL0

(Reset Value 0000 0000)

XOON	Enable 4fsc (XI / XO) oscillation and input of VDIN	0 : Disable 1 : Enable	R/W
S / N	Y/C separate output (SC and SY)	0 : Disable 1 : Enable	

P4 port Mode Register

P4MR (F785H)

7	6	5	4	3	2	1	0
AFFMIX	SCLK1E	RXD1E	SWPE	BLKE	TXD1E	RGBE	DOTXE

(Reset Value 0000 0000)

RGBE	R/G/B Output Enable	0 : Disable 1 : Enable	R/W
DOTXE	DOTXI, DOTXO Oscillation Enable	0 : Disable 1 : Enable	

CSYNC Control Register

CSYNCR (FFFDH)

7	6	5	4	3	2	1	0
AVDPO	AHDPO	MDET1	MDET0	SYNCDET	HSEN	MASK	

(Reset Value 0010 0000)

AVDPO	External VDIN Input Porarity Switch	0 : Positive 1 : Inverted	R/W
AHDPO	External HDIN (P44) Input Porarity Switch	0 : Positive 1 : Inverted	

(3) Display RAM

Display RAM locates indirect address 000H to 0EFH which is accessed by using OSDADR.

Display RAM (character code register)

	9	8	7	6	5	4	3	2	1	0
CHARD0 (00H)	OSDCR <CMD1>	OSDCR <CMD0>	CHARD0<CD7 to CD0>							
to						to				
CHARD239 (EFH)	OSDCR <CMD1>	OSDCR <CMD0>	CHARD239<CD7 to CD0>							

CD7 to CD0	Character code (252 character code + 4 blank code : 00H to FFH)	write only

The character displaying position on TV screen corresponds to the display RAM address. The RAM data corresponds to a displayed character (Character code: CD7-CD0) on TV screen.

Fig.3.16.2 shows the relation between Display RAM address and Display position on TV screen.

TV Screen Top / Left — 24 CHARACTERS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
2	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
3	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F	40	41	42	43	44	45	46	47
4	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
5	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77
6	78	79	7A	7B	7C	7D	7E	7F	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
7	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
8	A8	A9	AA	AB	AC	AD	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
9	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7
10	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF

10 lines

Screen Bottom / Right

Note) The number in each square indicates the address for RAM (hexadecimal notation)

Fig. 3.16.2 Relation between Display RAM address and Display position

The display RAM can be accessed indirectly through OSD RAM address register (OSDADR) and OSD data buffer register (OSDDBR). Write the OSD RAM address in OSDADR and its data in OSDDBR. As the data of OSDADR is incremented automatically when the character data is written in OSDDBR, only the initial address should be written in case that the continuous RAM addresses are accessed.

Data length of OSD display RAM is 10 bit. The lower 8 bits represent a character code (00H to FBH) or blank code (FCH to FEH) and are written the contents of OSDDBR by writing data to OSDDBR. Background of screen (Blank) is displayed when the blank code is written. The upper 2 bits represent a blinking mode (Display style) and are written the contents of OSD control register OSDCR (CMD1, CMD0) when the OSDDBR is accessed.

Following is an example of display RAM data setting.

```
LD (OSDCR), 00110000B    ;  <CMD1, 0> = 00, <TCEN> = 1, <DISPON> = 1
LD (OSDADR), 00000000B   ;  RAM address = 00H (Initializing Address counter)
LD (OSDDBR), 00000000B   ;  Character code = 00H (at RAM address = 00H), Upper 2 bit of
                            RAM = 00
LD (OSDCR), 11110000B    ;  <CMD1, 0> = 11
LD (OSDDBR), 00000010B   ;  Character code = 02H (at RAM address = 01H),
                         ;  Upper 2 bit of RAM = 11
LD (OSDCR), 00110000B    ;  <CMD1, 0> = 00
LD (OSDDBR), 00000101B   ;  Character code = 05H (at RAM address = 02H),
                         ;  Upper 2 bit of RAM = 00
```

<Caution about writing data into display RAM>

The display RAM data are read out by OSD at the specific timing synchronized with HD. Therefore, the data writing from CPU must be done at the different timing of data reading. In order to prevent this conflict, data writing interval to display RAM must be longer than TORW (s) shown below.

$T_{ORW} = 8/fc + 5n/f_{TC}$ [s]

fc : Main clock frequency (XIN / XOUT)
f_{TC} : Dot clock frequency
(Refer to Chapter 3.16.4: Display mode)
n : Character size for horizontal (n = 1, 2, 3, 4)

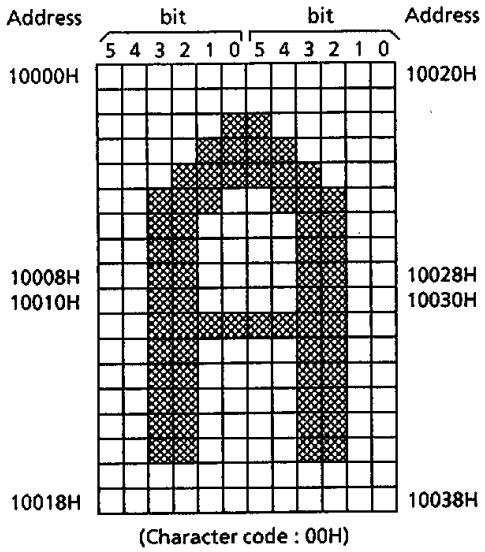
Note) Data writing here means a write cycle of Bus Operation.
Refer to Chapter 2: TLCS-90 CPU for the Bus operation of each instructions.

Also, the interval from accessing OSDDBR to accessing OSDADR should be longer than TORW (s). But, there are no ristriction for the interval from accessing OSDADR to accessing OSDDBR. (Accessing here means a write or read cycle of Bus operation.)

(4) Character ROM

Character ROM consists of 12dots (6 + 6 = 12 bits) in horizontal and 18dots (9 + 9 = 18 bits) in vertical, totally 216 dots and keeps 256-character font. This ROM is assigned from address 10000H to 13FFFH. Data "1" means display and "0" means non-display.

The bit address, data and character image is shown as the follows (as character code "00H"). Similarly as character code "00H", address 10040H to 10078H is assigned for character code "01H", address 10080H to 100B8H is assigned for character code "02H".



Address	Data	Address	Data
10000H	C0H	10020H	C0H
10001H	C0H	10021H	C0H
10002H	C1H	10022H	E0H
10003H	C3H	10023H	F0H
10004H	C7H	10024H	F8H
10005H	CEH	10025H	DCH
10006H	CCH	10026H	CCH
10007H	CCH	10027H	CCH
10008H	CCH	10028H	CCH
10010H	CCH	10030H	CCH
10011H	CFH	10031H	FCH
10012H	CCH	10032H	CCH
10013H	CCH	10033H	CCH
10014H	CCH	10034H	CCH
10015H	CCH	10035H	CCH
10016H	CCH	10036H	CCH
10017H	C0H	10037H	C0H
10018H	C0H	10038H	C0H

Fig 3.16.3 Character "A" as Code "00H"

Note 1) If actual font is full size of character font area, unexpected fringe is generated when fringe is enabled. Design character font carefully.

Note 2) TMP90PR74A, OTP device Character ROM:
Character ROM locates from memory address 10000H to 13FFFH. The PROM writer need to write up to 1Mbit. Since character data have 6bits for single address, upper 2-bit of 8-bit (non-used bits) should be "11" for OTP device.

Note 3) If the TMP90CR74A is used for the set lacking OSD function, set whole area of character ROM to "C0H".

3.16.4 Display Mode

(1) Internal Sync mode (Full page mode)

Full page mode is an internally synchronized mode, in which the sync signal (HD and VD) of the OSD is generated from the 4fsc signal in sync generator. It can be used, for example, in displaying a blue background, or in the display screen used in programming a VCR.

Full page mode is selected by resetting <EXT / $\overline{INT}$> bit in OSDCR register to "0".

(2) External sync mode (Super-impose mode)

Super-impose mode is an external sync mode synchronizing an external sync signal (HD and VD) inputted from port. It can be used for superimposing a message or other text on a play-back or broadcast (EE) display. Timing of the superimposition is determined by the BLK signal (P42 (BLK) terminal or PV / BLK terminal). (Switching between the superimposed and the background signal is carried out externally by using this BLK signal.)

Super-impose mode is selected by setting <EXT / $\overline{INT}$> bit in OSDCR register to "1". In this mode, the background display is a play-back display or an EE display.

Note : Since character coloring is not supposed in this mode, it is essential that coloring of back ground, character back ground and characters should be turned off, otherwise the superimposed text will be difficult to read.

The structure of the display on TV screen is shown in Fig 3.16.4.

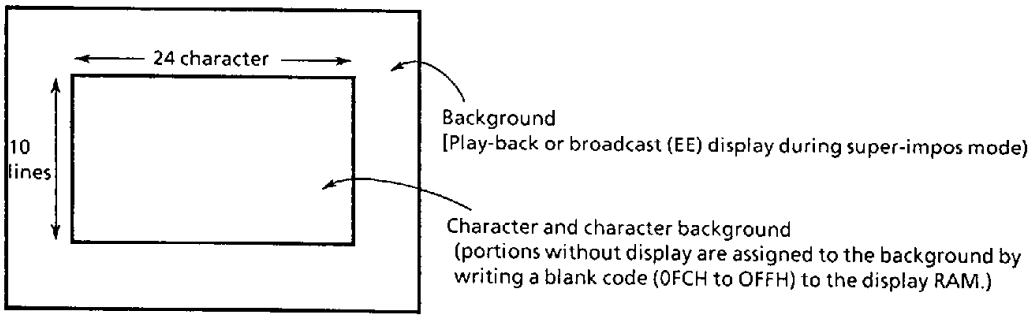


Fig 3.16.4 TV Screen Display

(3) Configuration of OSD Clock Generator

The OSD clock generator consists of clock generators for 4fsc clock and dot clock. Fig.3.16.5 shows a configuration of OSD clock generator.

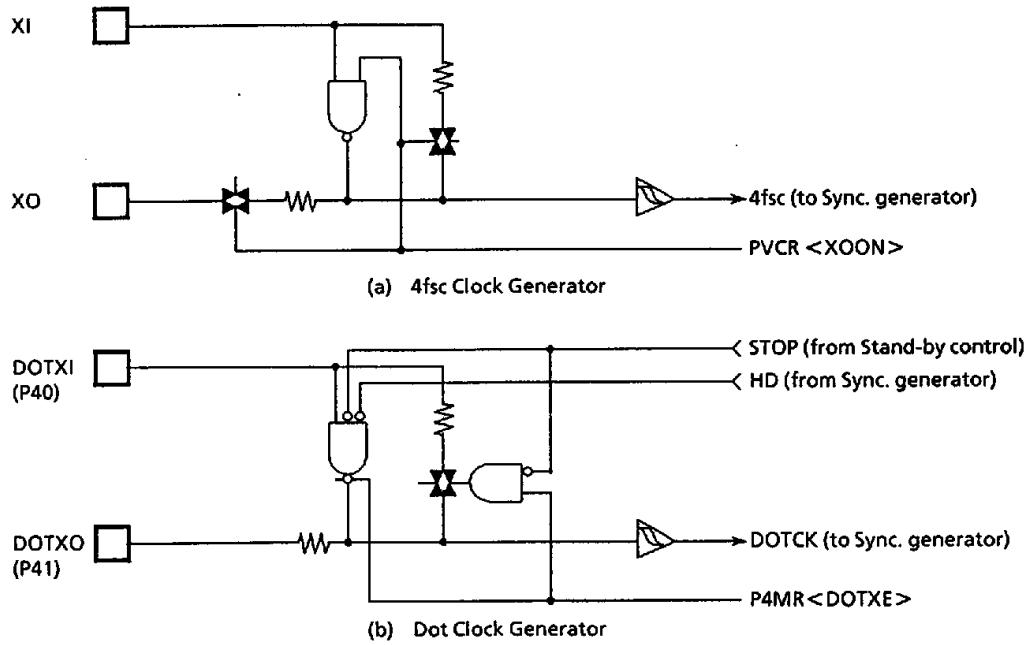
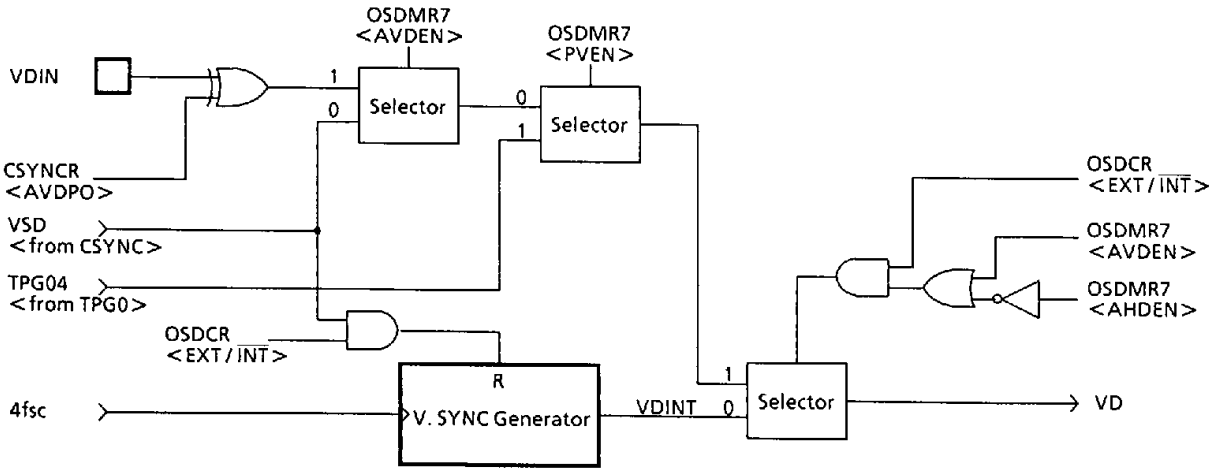


Fig 3.16.5 Configuration of OSD Clock Generator

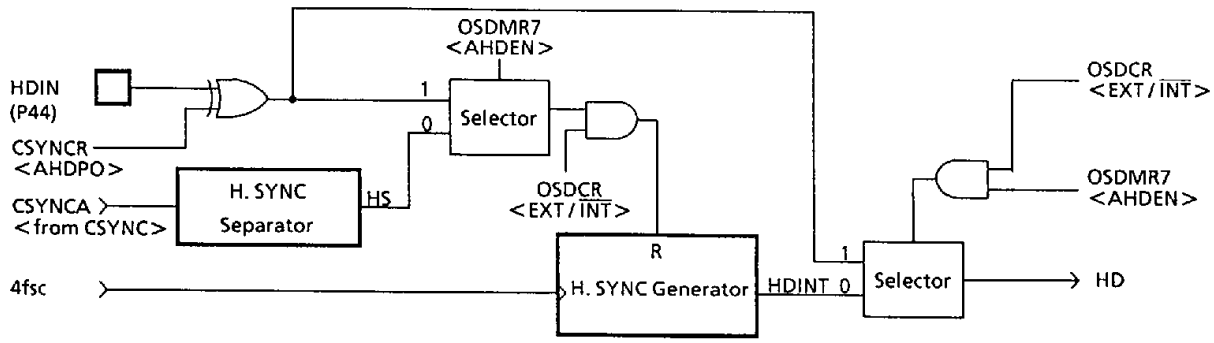
(4) Configuration of Sync. Generator

The sync. generator generates a Vertical Driving signal (VD), Horizontal Driving signal(HD) and horizontal dot-clock (TC) by using 4fsc clock (4 times frequency of color Sub-Carrier) and Dot-clock (DOTCK) from OSD clock generator.

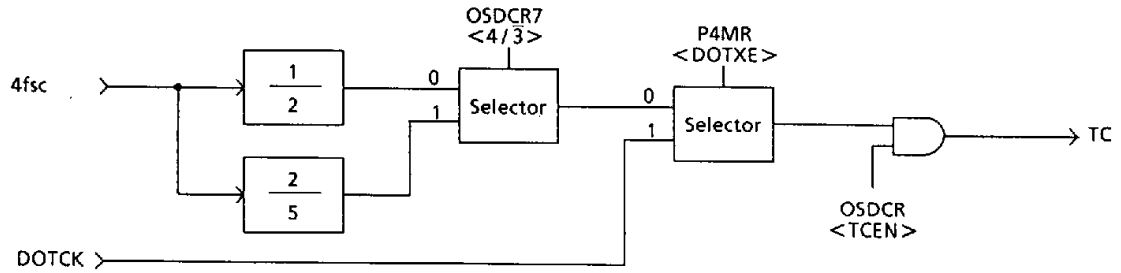
Fig.3.16.6 shows a configration of Sync. Generator.



(a) Generation circuit for Vertical Driving signal (VD)



(b) Generation circuit for Horizontal Driving signal (HD)



(c) Generation circuit for dot-clock (TC)

Fig 3.16.6 Configuration of Sync. Generator

(5) Source signal selection for VD and HD

① Source signal for VD

The source signal of VD can be selected from followings by setting the OSD Control Register (OSDCR <EXT/$\overline{INT}$>) and OSD Mode Register (OSDMR7 <AVDEN>, <AHDEN>, <PVEN>)

(a) VDINT: It is a V-sync. signal generated from prescaler of 4 fsc (V-sync. Generator). The VDINT is synchronized with follwing VSD signal in case of external sync. mode (<EXT/$\overline{INT}$> = "1").

(b) VDIN : It is a V-sync. signal inputted from VDIN terminal.

(c) VSD : It is a V-sync. signal separated from Composite Synchronizing signal by internal C-sync. separator.

(d) TPG04: It is an output signal from Timing Pulse Generator 0 (TPG0) used as a Pseudo V-sync. signal (PV) for special play-back.

② Source signal for HD

The source signal of HD can be selected from followings by setting the OSDCR <EXT/$\overline{INT}$> and OSDMR7<AHDEN>.

(a) HDINT : It is a H-sync. signal generated from prescaler of 4fsc (H-sync. Generator). The HDINT is synchronized with following HDIN or HS in case of external sync. mode (<EXT/$\overline{INT}$> = "1").

(b) HDIN : It is a H-sync. signal inputted from HDIN (P44) terminal.

(c) HS : It is a H-sync. signal separated from Composite-Sync. signal by internal C-sync. separator.

Table 3.16.2 shows a relationships between source signals of HD/VD and their register settings. (System matrix for HD and VD)

Table 3.16.2 System matrix for HD and VD

Display Mode	OSDCR <EXT/$\overline{INT}$>	OSDMR7 <AVDEN>	OSDMR7 <AHDEN>	OSDMR7 <PVEN>	HD	VD
Internal Sync Mode	0	*	*	*	HDINT	VDINT
External Sync Mode	1	0	0	0	HDINT (HS)	VSD
				1		TPG04
		0	1	0	HDIN	VDINT (VSD)
				1		
		1	0	0	HDINT (HS)	VDIN
				1		TPG04
		1	1	0	HDIN	VDIN
				1		TPG04

Note: (HS) ; Synchronized with HS, (VSD) ; Synchronized with VSD

(6) Selection of Dot-Clock(TC)

The horizontal dot-clock (TC) can be selected from either the output of dot-clock oscillation circuit (DOTXI/DOTXO) or prescaler output of 4fsc.

The output of prescaler (4fsc / 2 or 2 × 4fsc / 5) can be selected by setting of the OSD Control Register (OSDCR<4/3>) when a dot clock is disable (P4MR<DOTXE> = "0").

A horizontal synchronizing jitter is 4fsc/2 (Hz) when the dot clock is produced from the output of 4fsc prescaler.

(7) Correspondance between a register setting and Video system in internal sync. mode (Full page mode)

The correspoding Video system (PAL / NTSC) can be selected by setting the OSD Control Register (OSDCR<4/$\overline{3}$>, <50/$\overline{60}$>, <P/$\overline{N}$> in the internal sync. mode (Full page mode). The OSD coloring is not suported in external sync. mode (Super-imposed mode).

Table 3.16.3 shows a register setting for corresponding Video system.

<4/$\overline{3}$>	Setting for Color sub-carrier frequncy (fsc)	0 : 3.58 MHz 1 : 4.43 MHz
<50/$\overline{60}$>	Setting for V-sync. frequency (fv)	0 : 60 Hz 1 : 50 Hz
<P/$\overline{N}$>	Setting for Coloring system	0 : NTSC 1 : PAL

Table 3.16.3 Register setting for corresponding Video system

<4/$\overline{3}$>	<50/$\overline{60}$>	<P/$\overline{N}$>	Video system
0	0	0	NTSC
0	1	0	–
1	0	0	4.43 NTSC
1	1	0	–
0	0	1	M - PAL
0	1	1	N - PAL
1	0	1	60 PAL
1	1	1	PAL

(8) Interlace and Non-interlace Display

The frequency ratio between the Vertical Driving signal (VD) and Horizontal Driving signal (HD) genenated in internal sync. (Full-page) mode can be selected in the following way. The HD / VD ratio is determined by setting OSD control register (OSDCR<50/$\overline{60}$>) and OSD mode register 7 (OSDMR7 <NONINT>, <RATIOHV>).

<50/$\overline{60}$>	0	0	0	0	1	1	1	1
<NONINT>	0	0	1	1	0	0	1	1
<RATIOHV>	0	1	0	1	0	1	0	1
HD/VD	262.5	263.5	263.0	264.0	312.5	313.5	313.0	314.0

Setting OSDMR7<EQON> to "1" adds a serrated pulse and an equalizing pulse during the Vertical blanking interval.

3.16.5 Display Position

(1) Start position in horizontal line

The start position can be selected from 16-positions every 4 dots (Tc) by <POSH3 > - <POSH0> bits in OSDMR0 register.

The actual position can be calculated by following form.

$$Hposi = Tc \times (4 \sum_{n=0}^{3} 2^n \cdot POSHn + NH)$$

Tc is the period of dot clock.
POSHn is the value in <POSH3> to <POSH0>.
NH is the variable depends on character size in horizontal.

Horizontal Size of Character	NH
x 1 (1TC/1 dot)	43
x 2 (2TC/1 dot)	53
x 3 (3TC/1 dot)	63
x 4 (4TC/1 dot)	73

(2) Start position in vertical line

The start position can be selected from 16-positions every 4 HD by <POSV3> - <POSV0> bits in OSDMR0 register.

The actual position can be calculated by following form.

$$Hposi = TH \times (4 \sum_{n=0}^{3} 2^n \cdot POSVn + NV)$$

TH is the period of horizontal sync signal.
POSVn is the value in <POSV3> to <POSV0>.
NV is the variable depends on character size in vertical.

Vertical Size of Character	NV
x 1 (1TH/1 dot)	5
x 2 (2TH/1 dot)	6
x 3 (3TH/1 dot)	7
x 4 (4TH/1 dot)	8

3.16.6 Display Size

The size of display characters can be selected 1 to 4 times in both horizontal and vertical, total combination is 16 sizes.

The first line can be set its special size independently from other lines.

(1) 1st line character size

The size of 1st line can be set by <FSV1, FSV0> and <FSH1, FSH0> bits in OSDMR1 register.

<FSV1>	<FSV0>	Vertical Size
0	0	x 1
0	1	x 2
1	0	x 3
1	1	x 4

<FSH1>	<FSH0>	Horizontal Size
0	0	x 1
0	1	x 2
1	0	x 3
1	1	x 4

(2) General lines (2nd to 10th lines) character size

The size of general line can be set by <CSV1, CSV0> and <CSH1, CSH0> bits in OSDMR1 register.

<CSV1>	<CSV0>	Vertical Size
0	0	x 1
0	1	x 2
1	0	x 3
1	1	x 4

<CSH1>	<CSH0>	Horizontal Size
0	0	x 1
0	1	x 2
1	0	x 3
1	1	x 4

3.16.7 Display Type

The display type of character is determined by the combination of character background and fringing, total four (4) types are available.

This display type can be set for 1st line and another Mth line to Nth line independently. Four types of character are shown in Fig 3.16.7.

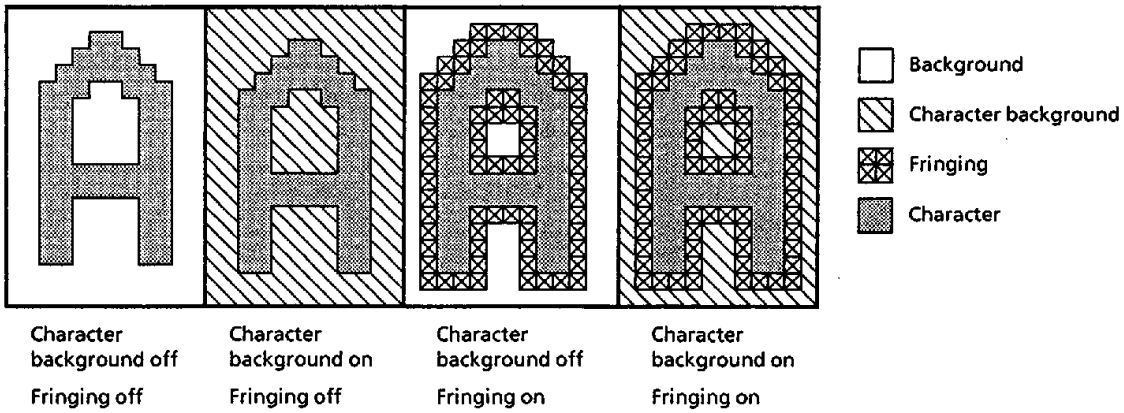


Fig 3.16.7 Display Character Type

(1) 1st line display type setting

The display type of 1st line can be set by <FLD1> and <FLD0> bits in OSDMR3 register.

<FLD1>	<FLD0>	Fringing	Character background
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	ON

(2) Mth to Nth lines display type setting

The display type of Mth to Nth lines can be set by <NLD1> and <NLD0> bits in OSDMR3 register.

<NLD1>	<NLD0>	Fringing	Character background
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	ON

The line number Mth and Nth are set by OSDMR2 register. The actual lines are calculated by following forms.

$$M = \sum_{n=0}^{3} 2^n \cdot MSLn + 1$$

$$N = \sum_{n=0}^{3} 2^n \cdot NSLn + 1$$

MSLn is the value in <MSL3> to <MSL0> bits in OSDMR2 register.
NSLn is the value in <NSL3> to <NSL0> bits in OSDMR2 register.

Caution : The value write into NSLn should be larger than or equal to MSLn ($M \leqq N$) and both value should not be exceeded ten (10). In case that N is equal to M, only one (1) line is designated; it's Nth (Mth). If M is equal to 1, designation begins on 2nd line and 1st line is set by <FLDn>.

(3) Other lines display type setting

The display type of other lines can be set by <GLD1> and <GLD0> bits in OSD Mode register3 (OSDMR3).

<GLD1>	<GLD0>	Fringing	Character background
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	ON

3.16.8 Line space

Line spacing is a function that sets the space between lines. Four types of spacing can be set using <SPACE1, SPACE0> bits in OSD mode register3 (OSDMR3). This setting controls the spacing of all 10 lines uniformly. (Only the line spacing of special lines can not be set) Settings are as follows,

<SPACE1>	<SPACE0>	
0	0	No space
0	1	1 dot (1 HD)
1	0	2 dots (2 HD)
1	1	4 dots (4 HD)

3.16.9 Smoothing and fringing

(1) Smoothing function

Smoothing is a function that corrects dot resolution when characters are enlarged, rendering the characters easier to read. It can be turned on/off by setting <SMOOTH> bit in OSD mode register7 (OSDMR7). This setting is valid when the character enlargement multiple is an even integer for both vertical and horizontal (i.e. V x H = 2 x 2, 2 x 4, 4 x 2 and 4 x 4).
The correction is one (1) dot when the multiple is two (2) and two (2) dots when the multiple is four (4).

(2) Fringing function

The border is an area surrounding a character to which a black level signal has been added, and which is a single dot wide irrespective of the enlargement multiple of the character. When the smoothing is enabled, fringing is executed for area inclusive of dots corrected by smoothing.
Fig 3.16.8 shows the smoothing and Fringing display.

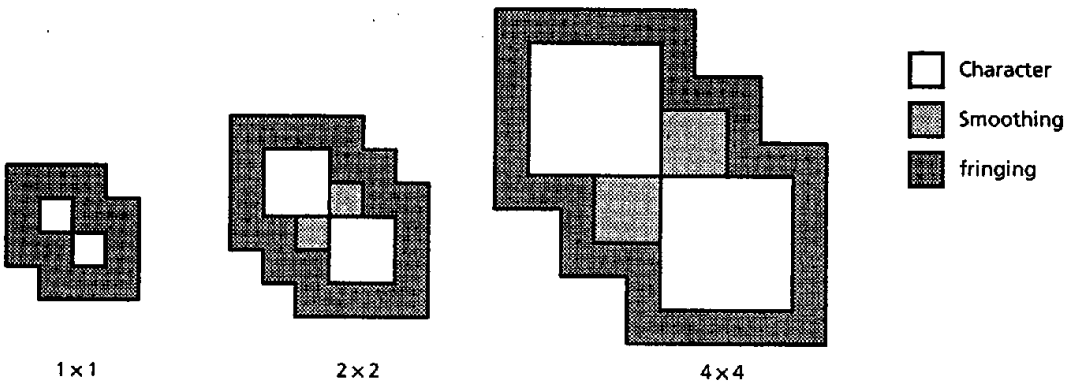


Fig 3.16.8 Smoothing and Fringing Function

3.16.10 Blinking

Three basic blinking modes, Standard, Reverse and Alternating, can be selected by <CMD1, 0> bits in OSD control register (OSDCR) loaded in two most significant bits of 10-bit display RAM data and <MOD> bit in OSD mode register (OSDMR4). Display modes corresponding to the setting of <MOD>, <CMD1> and <CMD0> are as follows,

Table 3.16.4 Blinking display mode

Display mode	<MOD>	<CMD1>	<CMD0>	Display
Standard characters	*	0	0	A ←→ A
Standard blinking	*	0	1	←→ A
Reverse character	*	1	0	**A** ←→ **A**
Reverse blinking	0	1	1	←→ **A**
Alternating blinking	1	1	1	**A** ←→ A

Set no line-space by setting OSDMR4 <SPACE1, SPACE0> = "00", when Reverse character or Reverse blinking or Alternating blinking is used.

Four blinking duty factors can be selected using <BLINK1> and <BLINK0> in OSD mode register4 (OSDMR4).

<BLINK1>	<BLINK0>	Duty factor
0	0	Blinking off
0	1	50 % (display off 50 % of time)
1	0	75 % (display off 25 % of time)
1	1	25 % (display off 75 % of time)

Two blinking periods, 1/64 and 1/32 of VD (approx. 1.0 [s] and 0.5 [s]), can be selected using <BLINK2> bit in OSD mode register4 (OSDMR4).

3.16.11 Coloring (Hue (Tint), Value (Luminance))

Selection can be made from eight (8) hues and five (5) level of luminance. Hue selection can be made independently for background, character background and characters. Setting for luminance applies to the entire screen, but when coloring is turned off, luminance can be set in five levels independently for each. Particularly that if coloring is turned off for all three (background, character background and characters), a monochrome video signal without color bursts is outputted.

(1) Coloring for Background

The hue of the background, and whether coloring is on or off for it, is specified by <BGOFF> and <BGPH2 - 0> bits in OSDMR5 register. The setting is follows,

<BGOFF>	<BGPH2>	<BGPH1>	<BGPH0>	Color phase angle (B-Y reference)	
				NTSC phase angle	PAL phase angle
0	0	0	0	45°	315° / 45°
0	0	0	1	270°	90° / 270°
0	0	1	0	135°	225° / 135°
0	0	1	1	180°	180°
0	1	0	0	0°	0°
0	1	0	1	315°	45° / 315°
0	1	1	0	90°	270° / 90°
0	1	1	1	225°	135° / 225°

<BGOFF>	<BGPH2>	<BGPH1>	<BGPH0>	Luminance
1	*	0	0	5 IRE
1	0	0	1	15 IRE
1	1	0	1	35 IRE
1	*	1	0	65 IRE
1	*	1	1	100 IRE

Note) When the background coloring is off (<BGOFF> = "1"), the luminance level of background can be selected by setting <BGPH2 - BGPH0>.

(2) Coloring for character background

The hue of the character background, and whether coloring is on or off for it, is specified by <CBOFF> and <CBPH2 to 0> bits in OSDMR5 register. The setting is follows,

<CBOFF>	<CBPH2>	<CBPH1>	<CBPH0>	Color phase angle (B-Y reference)	
				NTSC phase angle	PAL phase angle
0	0	0	0	45°	315°/45°
0	0	0	1	270°	90°/270°
0	0	1	0	135°	225°/135°
0	0	1	1	180°	180°
0	1	0	0	0°	0°
0	1	0	1	315°	45°/315°
0	1	1	0	90°	270°/90°
0	1	1	1	225°	135°/225°

<CGOFF>	<BGPH2>	<BGPH1>	<BGPH0>	Luminance
1	*	0	0	5 IRE
1	0	0	1	15 IRE
1	1	0	1	35 IRE
1	*	1	0	65 IRE
1	*	1	1	100 IRE

(3) Coloring for character

The hue of the characters, and whether coloring is on or off for it, is specified by <CFOFF> and <CFPH2 to 0> bits in OSDMR7 register. The setting is follows,

<CFOFF>	<CFPH2>	<CFPH1>	<CFPH0>	Color phase angle (B-Y reference)	
				NTSC phase angle	PAL phase angle
0	0	0	0	45°	315°/45°
0	0	0	1	270°	90°/270°
0	0	1	0	135°	225°/135°
0	0	1	1	180°	180°
0	1	0	0	0°	0°
0	1	0	1	315°	45°/315°
0	1	1	0	90°	270°/90°
0	1	1	1	225°	135°/225°

<BGOFF>	<BGPH2>	<BGPH1>	<BGPH0>	Luminance
1	*	0	0	5 IRE
1	0	0	1	15 IRE
1	1	0	1	35 IRE
1	*	1	0	65 IRE
1	*	1	1	100 IRE

(4) Value (Luminance)

The luminance level (Y) of the entire screen is specified by <YL2 to 0> in OSDMR6 register.

<YL2>	<YL1>	<YL0>	Luminance level
0	0	*	5 IRE
0	1	0	15 IRE
0	1	1	35 IRE
1	0	*	65 IRE
1	1	*	100 IRE

(5) Coloring Change by Blank code

Blank code (display RAM data 0FCH to 0FFH) can be used to change the hue of the characters or the character background within a single screen. Setting a blank code from 0FCH to 0FEH changes the hue of the character or the hue of the character background following that blank, and setting a blank code 0FFH returns the hue of it following that blank to the initial value (value in <CFPH2 to 0> or <CBPH2 to 0>).

When a blank code from 0FCH to 0FEH is set, hue PH0 and PH1 are changed to three different combinations with respect to the initial value, and hue PH2 is changed to the value set in <FCPH2>, <FDPH2> and <FEPH2> bits in OSDMR4 register. The ways in which the settings change as a result of blank codes when the initial settings for <CFPH2, CFPH1, CFPH0> are (CF2, CF1, CF0), <CBPH2, CBPH1, CBPH0> are (CB2, CB1, CB0) are as follows,

when <CB / $\overline{CF}$> = "0" (change the hue of character)

Blank code	Hue of Character			
	PH2	PH1	PH0	
0FCH	FCPH2	$\overline{CF1}$	$\overline{CF0}$	CF0, CF1 are reversed
0FDH	FDPH2	CF1	$\overline{CF0}$	Only CF0 is reversed
0FEH	FEPH2	$\overline{CF1}$	CF0	Only CF1 is reversed
0FFH	CF2	CF1	CF0	Return to initial value

when <CB / $\overline{CF}$> = "1" (change the hue of the character background)

Blank code	Hue of Background of Character			
	PH2	PH1	PH0	
0FCH	FCPH2	$\overline{CB1}$	$\overline{CB0}$	CB0, CB1 are reversed
0FDH	FDPH2	CB1	$\overline{CB0}$	Only CB0 is reversed
0FEH	FEPH2	$\overline{CB1}$	CB0	Only CB1 is reversed
0FFH	CB2	CB1	CB0	Return to initial value

3.16.12 SC / SY Output

For supporting S terminal of S-VHS, OSD can output SC (chroma signal) and SY (luminance signal), respectively from P46 and P47 terminals. Setting <S/N> bit in PVCR register to "1" will generate output of SC / SY.

Output amplitude of SC is 1Vp-p (typ.) and that of SY (in case of 100% white) is 2Vp-p. Therefore, external level matching is necessary.

3.16.13 R/G/B output

The OSD can output R/G/B signal as a component Video output in addition to the composite Video output. The R/G/B signal is a combination of logic levels corresponding to the hue for the background, character background and character. They are outputted from P45, P46 and P47.

SC / SY output must be disabled during RGB output. By setting <RGBEN> bit in P4MR register to "1", above terminals can be set as RGB output.

3.17 SERIAL CHANNELS (SIO0 / SIO1)

The TMP90CR74A has two built-in 8-bit synchronous serial channels. Serial channel 0 (SIO0) is connected to an external circuit via P25 (SCLK0), P26 (TXD0), P27 (RXD0), and serial channel 1 (SIO1) is connected to an external circuit via P57 (SCLK1), P42 (TXD1), P45 (RXD1). To use SIO function, set the mode register P2MR (P4MR for channel 1) to SIO pin function. Serial channel 0 and 1 are identical circuits, configured independently.

3.17.1 Configuration

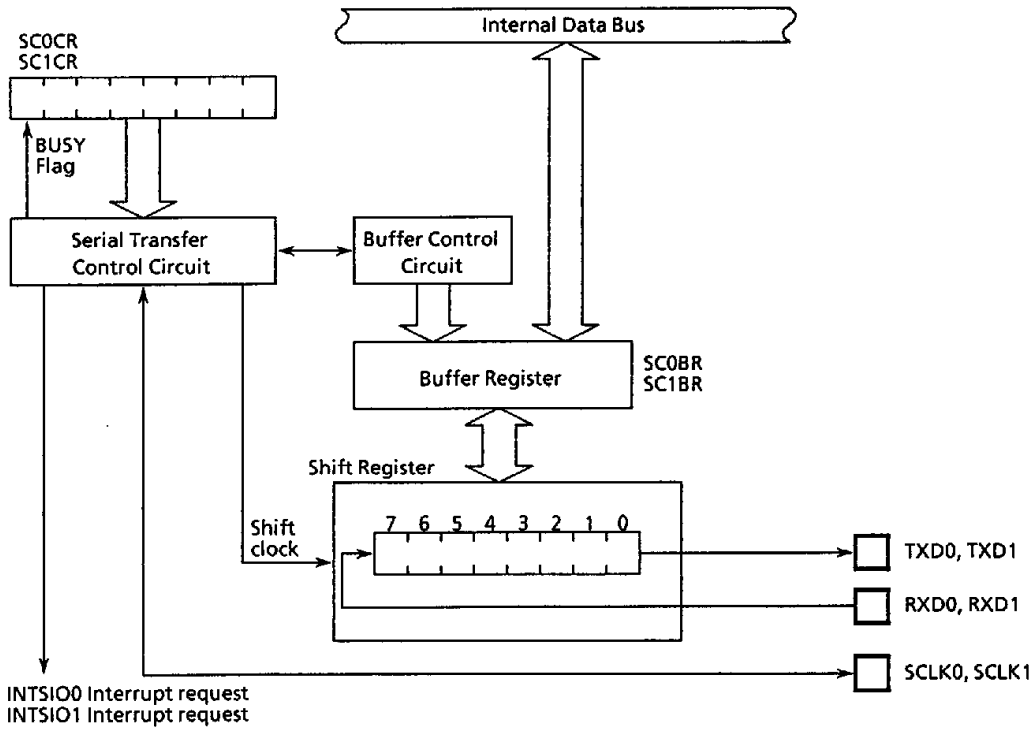


Fig 3.17.1 Configuration of Serial Channel

3.17.2 Control Registers

The serial channels are controlled by two (2) control registers SC0CR, SC1CR and two (2) buffer registers SC0BR, SC1BR.

Serial Channel 0 Control Register

SC0CR (FFDFH)

7	6	5	4	3	2	1	0
FF0SI	S0RES	S0MD1	S0MD0	SIFT0	CLK0SI	SCK0S	SIO0E

(Reset Value 1000 0000)

FF0SI	Serial transfer monitor flag	0 : Transfer in progress 1 : Stop transfer	read only
S0RES	Serial transfer transfer terminate	0 : – 1 : Terminate (one-shot)	R/W
S0MD1 S0MD0	Serial transfer mode select	00 : Transmit mode 01 : Receive mode 10 : – 11 : Transmit / receive mode	
SIFT0	Serial transfer shift edge select	0 : Leading (Falling) edge 1 : Trailing (Rising) edge	
CLK0SI	Serial internal clock rate select	0 : TBC4 1 : TBC7	
SCK0S	Serial transfer clock select	0 : Internal clock 1 : External clock	
SIO0E	Serial transfer enable / disable	0 : Disable 1 : Enable	

Serial Channel 0 Buffer Registe

SC0BR (FFDEH)

7	6	5	4	3	2	1	0
TRB07	TRB06	TRB05	TRB04	TRB03	TRB02	TRB01	TRB00

(Initial Value **** ****) (R/W)

Serial Channel 1 Control Register

SC1CR (FFE1H)

7	6	5	4	3	2	1	0
FF1SI	S1RES	S1MD1	S1MD0	SIFT1	CLK1SI	SCK1S	SIO1E

(Initial Value 1000 0000)

FF1SI	Serial transfer monitor flag	0 : Transfer in progress 1 : Stop transfer	read only
S1RES	Serial transfer terminate	0 : – 1 : Terminate (one-shot)	R/W
S1MD1 S1MD0	Serial transfer mode select	00 : Transmit mode 01 : Receive mode 10 : – 11 : Transmit / receive mode	
SIFT1	Serial transfer shift edge select	0 : Leading (Falling) edge 1 : Trailing (Rising) edge	
CLK1SI	Serial internal clock rate select	0 : TBC4 1 : TBC7	
SCK1S	Serial transfer clock select	0 : Internal clock 1 : External clock	
SIO1E	Serial transfer enable / disable	0 : Disable 1 : Enable	

Serial Channel 1 Buffer Register

SC1BR (FFE0H)

7	6	5	4	3	2	1	0
TRB17	TRB16	TRB15	TRB14	TRB13	TRB12	TRB11	TRB10

(Initial Value **** ****) (R/W)

3.17.3 Operation

(1) Serial Clock

① Clock Source Selection

The clock of SIO can be selected from either external clock or internal clock by setting <SCK0S> bit in SC0CR register (<SCK1S> bit in SC1CR register for channel 1).

a. Internal clock

The clock rate can be selected from either TBC4 (25/fc) or TBC7 (28/fc) by setting <CLK0SI> (<CLK1SI> for channel 1). Table 3.17.1 shows the maximum transfer rate using the internal clock.

The serial clock automatically stops after the end of one-frame serial operation, and waits for the next serial operation. The serial clock holds high-level are not transferred.

Table 3.17.1 The Maximum Transfer Rate by Internal Clock

Internal Clock	Maximum Transfer Rate (at fc = 16 MHz)
TBC4 (2^5/fc)	500000 bps
TBC7 (2^8/fc)	62500 bps

b. External clock

.The clock input to the SCLK0 (SCLK1 for channel 1) pin is used as the serial clock. To make certain of the shift operation, set serial clock select register <SCL0S> (<SCL1S> for channel 1) to "1". Using certain shift operation, it is necessary to set more than 8/fc at both high-level and low-level of the serial clock width.

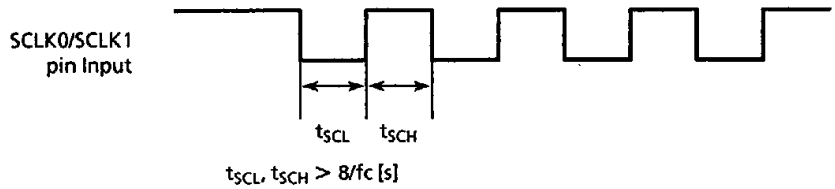


Fig 3.17.2 External Clock Input

② Shift Edge Selection

The leading or trailing edge shift can be selected by setting <SIFT0> bit in SC0CR register (<SIFT1> bit in SC1CR register for channel 1).

a. Leading edge

The serial data are shifted on the leading edge of the serial clock (falling edge of SCLK0 or SCLK1 pin input/output).

b. Trailing edge

The serial data are shifted on the trailing edge of the serial clock (rising edge of SCLK0 or SCLK1 pin input/output).

In the transmit mode, trailing edge mode can not be operating.

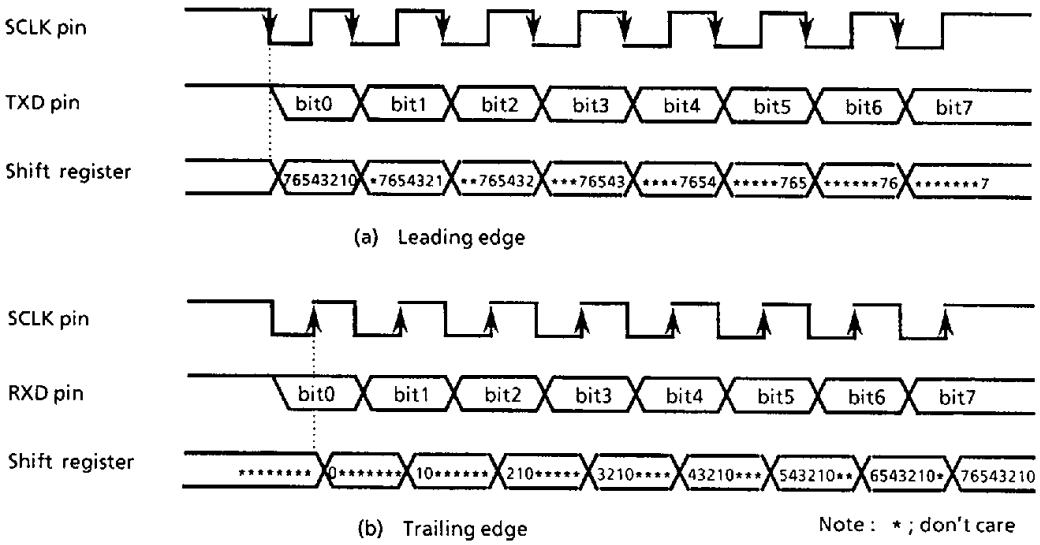


Fig 3.17.3 Shift Edge

(2) Serial Operation

Three transfer mode such as transmit, receive and simultaneous transmit-receive modes for serial channel 0 and 1 are selected by SC0CR<S0MD1, 0> (SC1CR<S1MD1, 0 for channel 1). After reset, SC0CR<S0MD1, 0> and SC1CR<S0MD1, 0> are cleared to "0", and transmit mode is selected. The following explains the operation in each transfer mode.

① Transmit mode

After setting transmit mode to the control register, the first transmit data is written into buffer registers SC0BR or SC1BR (address FFDEH or FFE0H in memory). (When transmit mode is not set, transmit data can not be written into the buffer registers.) Setting SC0CR<SIO0E> or SC1CR<SIO1E> to "1" starts transmit operation. As the transmit starts, the transmit data area synchronized with the leading edge of the serial clock (falling edge shift), and sequentially output from the TXD pin of the LSB side. At the same time, the transmit data area transferred from the buffer registers to the shift registers. Since the buffer registers are empty, the buffer empty interrupt (INTSIO0 or INTSIO1) is generated to request new data. When the next transmit data is written into the buffer register in the interrupt service program, the interrupt request signal is cleared.

Note : After the serial transfer enable/disable register SC0CR<SCO0E> or SC1CR<SIO1E> are set to "1", undefined data are output from TXD pin till the first falling edge of the serial clock.

(Internal clock mode)

In the internal clock mode, When all data are transmitted and no subsequent data is set in the register, the serial clock output stops and a wait begins.

Figure 3.17.4 (a) shows the timing chart of internal clock operation in transmit mode (with wait).

(External clock mode)

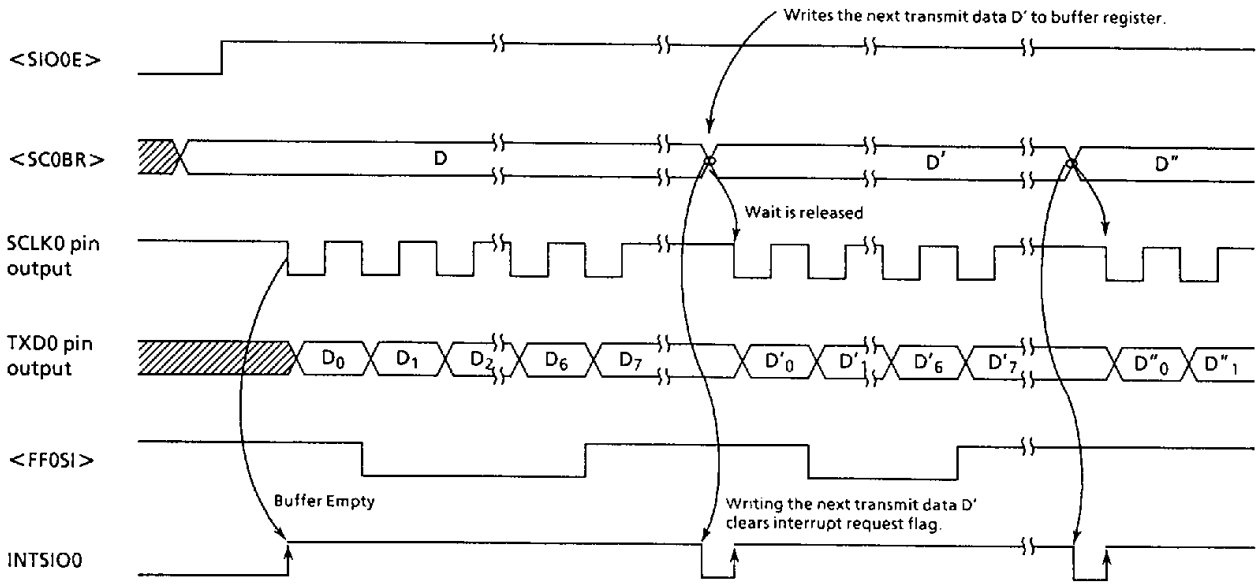
In the external clock mode, data must be set in the buffer registers before the next data shift operation begins. Therefore the transfer rate is determined by the maximum delay time from interrupt request generation to writing the transmit data into the buffer register in the interrupt service program.

Figure 3.17.4 (b) shows the timing chart of external clock operation in transmit mode.

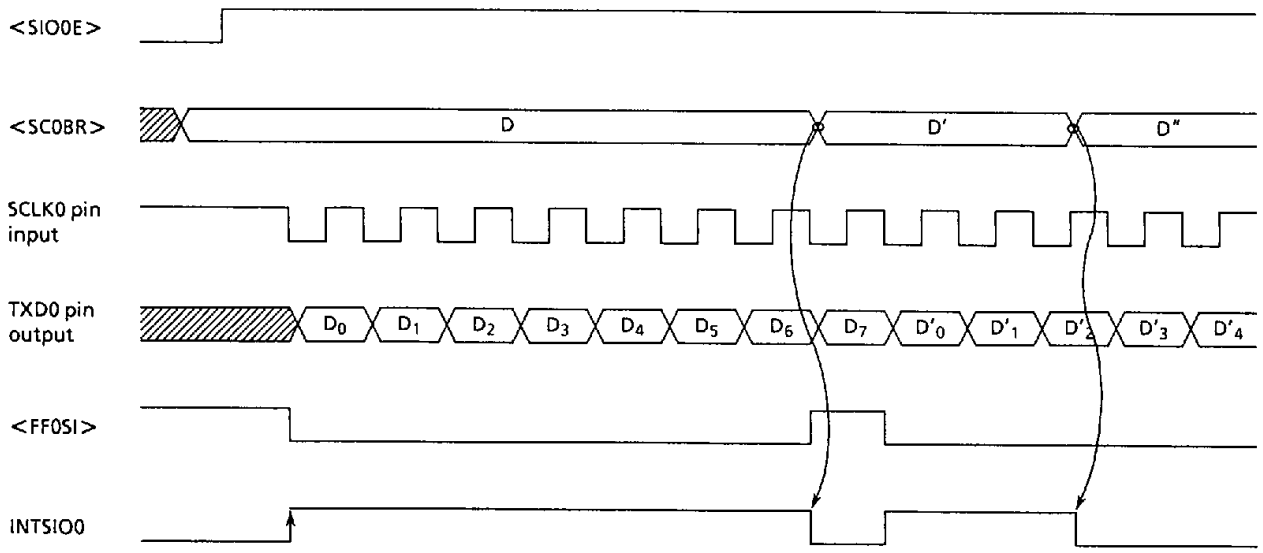
To end the transmit operation, set SC0CR<SIO0E> or SC1CR<SIO1E> to "0" instead of writing the next transmit data into the buffer register in the interrupt service program. When<SIO0E> or <SIO1E> are cleared to "0", the transmit operation stops at once by setting SC0CR<S0RES> or SC1CR<S1RES> to "1", and <S0RES> or <S1RES> are automatically cleared to "0".

The end of transmit operation can be confirmed by reading out the serial transfer monitor flag SC0CR<FF0SI> or SC1CR<FF1SI>. (When the transmit operation is finished, the serial transfer monitor flag is set to "1".)

In the external clock mode, the serial transfer enable/disable register<SIO0E> or <SIO1E> must be cleared to "0" before starting the next transmit data shift operation. If <SIO0E> or <SIO1E> is not cleared to "0" before the shift operation begins, operations stop after transferring the next transmit data (dummy).



(a) Internal clock operation in transmit mode (with wait)



(b) External clock operation in transmit mode

Fig 3.17.4 Serial channel Timing Chart in Transmit mode

② Receive Mode

After setting the control register to receive mode, setting SC0CR<SIO0E> or SC1CR<SIO1E> to "1" makes receive possible. The shift data is synchronized with the serial clock and fetched from the RXD pin. When 8-bit data is fetched, it is transferred from the shift register to the buffer register, and buffer-full interrupt INTSIO0 or INTSIO1 is generated to request a read of receive data. The receive data are read from the buffer register in the interrupt service program. The interrupt request signal is cleared when they are read.

(Internal clock mode)

In the internal clock mode, if the previous receive data has not been read from the buffer register after the next data is fetched, the serial clock stops and waits untill the previous data is read.

Figure 3.17.5 (a) shows the timing chart of internal clock operation in receive mode (leading edge shift with wait).

Figure 3.17.6 (a) shows the timing chart of internal clock operation in receive mode (trailing edge shift with wait).

(External clock mode)

In the external clock mode, as the shift operation synchronizes with supplied external clock, it is necessary to read from the buffer register before transferring the next receive data. If the previous data has not read,the receive data will not be transferred to the buffer register, and subsequent receive data will be canceled.

The maximum transfer rate of the external clock operation is determined by the maximum delay time from the generation of interrupt requests to receive data read.

Figure 3.17.5 (b) shows the timing chart of external clock operation in receive mode (leading edge shift).

Figure 3.17.6 (b) shows the timing chart of external clock operation in receive mode (trailing edge shift).

In the receive mode, either leading edge shift or trailing edge shift can be selected. Because data is fetched at the leading edge of the serial clock, the first shift data must already be input to the RXD pin when the initial serial clock pulses are applied at transfer start.

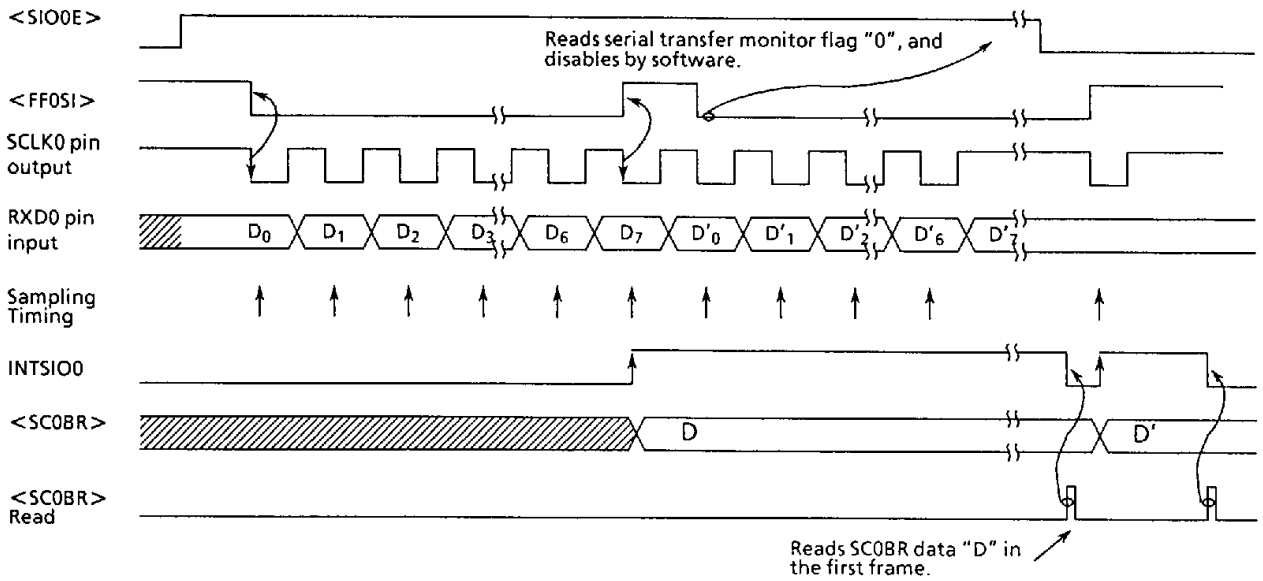
To end the receive operation, set the serial transfer enable/disable register (SC0CR)<SIO0E> or (SC1CR)<SIO1E> to "0". When the serial transfer enable/disable register <SIO0E> or <SIO1E> are cleared to "0", the receive operation ends after 8 bits of receive data are fetched and transferred to the buffer register.

Setting the serial transfer enable/disable register (SC0CR)<S0RES> or (SC1CR)<S1RES> are set to "1" stops the serial transfer at once and <SIO0E> or <SIO1E> are cleared to "0".

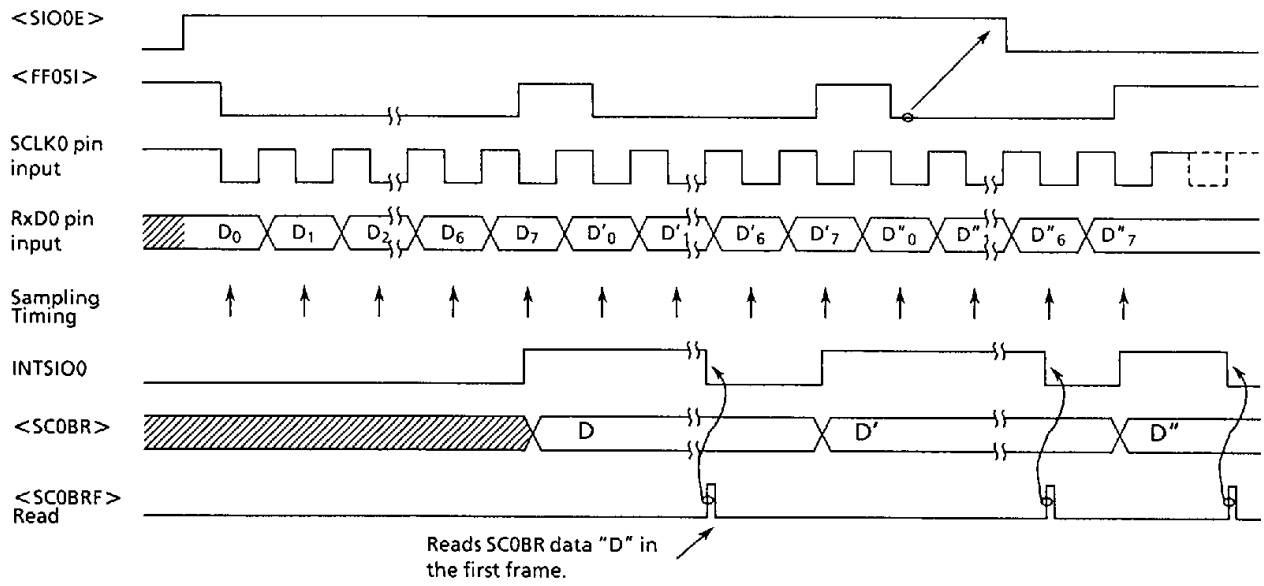
Note: If the transfer mode is switched, the contents of the buffer registers can not be kept. If necessary to switch the transfer mode, the transfer mode should be switched after clearing the transfer enable/disable register <SIO0E> or <SIO1E> to "0" and reading out the last bit of the receive data.

The end of receive can be confirmed by reading serial transfer monitor flags <FF0SI> or <FF1SI>.

An end of receive operation can be confirmed by reading the serial transfer monitor flag <FF0SI> or <FF1SI> in program.

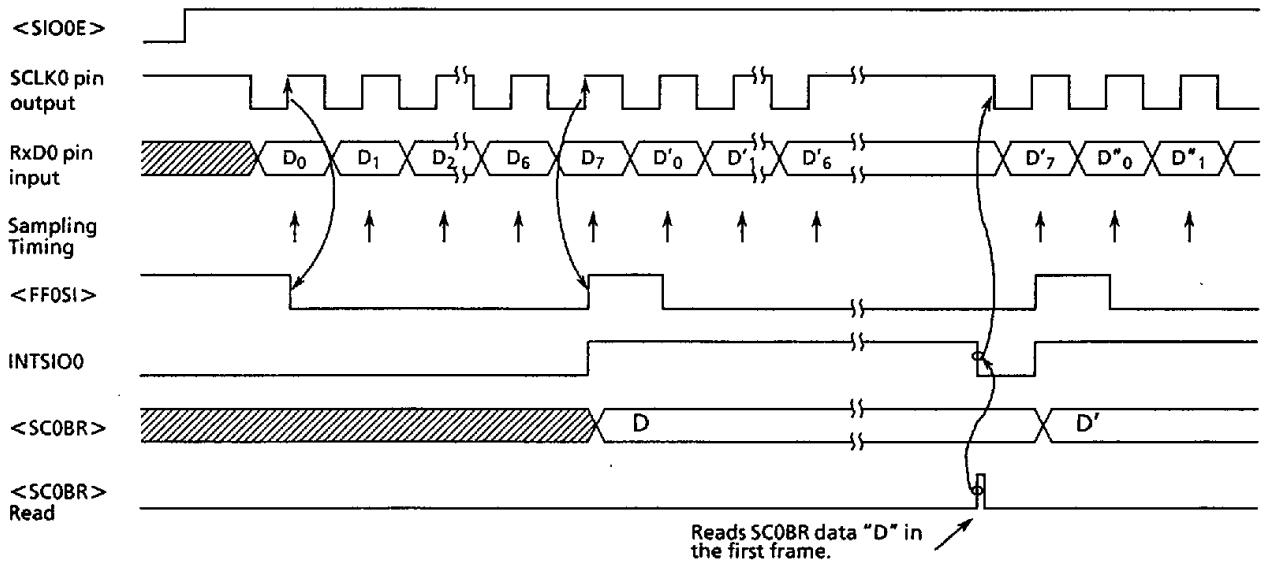


(a) Internal clock operation in receive mode (with leading edge and wait)

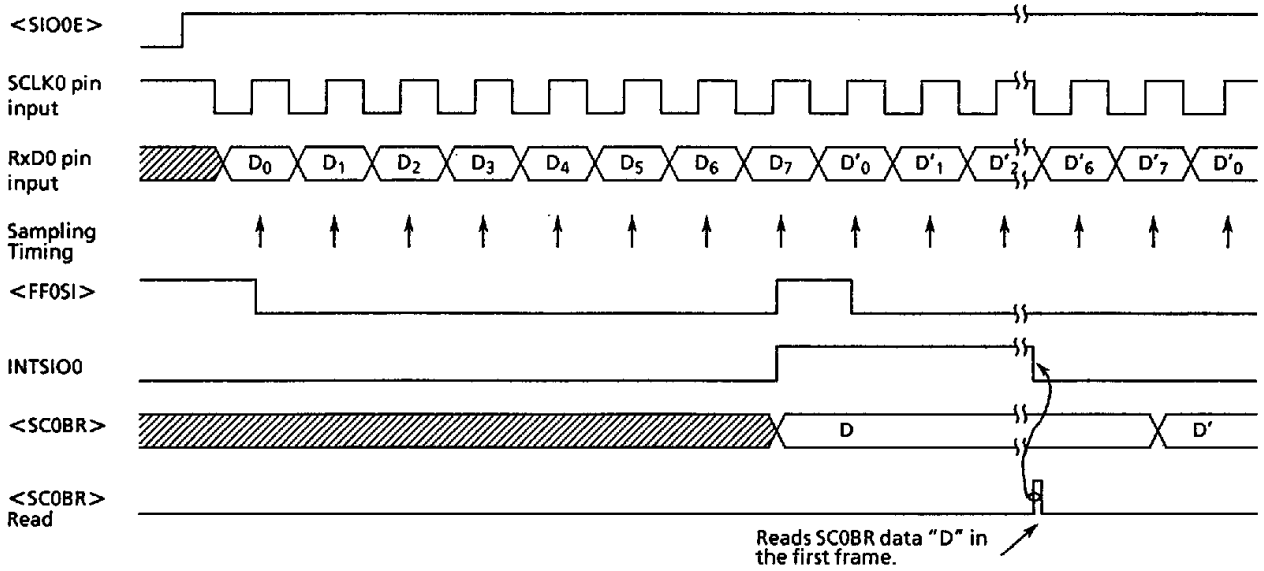


(b) External clock operation in receive mode (with leading edge)

Fig 3.17.5 Serial channel Timing chart in Receive mode (Leading edge)



(a) Internal clock operation in receicve mode (with trailing edge and wait)



(b) External clock operation in receive mode (with trailing edge)

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Fig 3.17.6 Serial channel Timing chart in Receive mode (Trailing edge)

③ Simultaneous Transmit / Receive Mode

The first transmit data are written into the buffer register SC0BR (SC1BR for channel 1) after the simultaneous transmit-receive mode is set to the control register. Then, setting the serial channel control register SC0CR<SIO0E> or SC1CR<SIO1E> to "1" enables transmitting or receiving data. The transmit data area output from the TXD pin at the leading edge of the serial clock. The receive data area fetched from the RXD pin at the trailing edge of the serial clock.

When the 8-bit receive data are fetched, the data are transferred from the shift register to the buffer register, and the interrupt request (INTSIO0 or INTSIO1) is generated to request receive data read. In the interrupt servise program, the received data are read out from the buffer register and the next transmit data are written into the buffer register.

Note : After the serial transfer enable/disable register SC0CR<SIO0E> or SC1CR<SIO1E> is set to "1", undifined data are output from TXD pin till the first falling edge of the serial clock.

(Internal clock mode)

In the internal clock mode, a wait begins until the receive data are read and the next transmit data are written into the buffer register.

(External clock mode)

In the external clock mode, the receive data must be read and the next transmit data written before the next shift operation, because the shift operation is synchronized with external supplied clock pulses. The maximum transfer rate of the external clock operation is detemined by the maximum delay time from interrupt request generation to receive data read and transmit data write.
Figure 3.17.7 (b) shows the timing chart of external clock operation in simultaneous transmit/receive mode.

Since the buffer registers are used for both transmit and receive data, always ensure that transmit data is written after 8 bits of receive data are fetched.

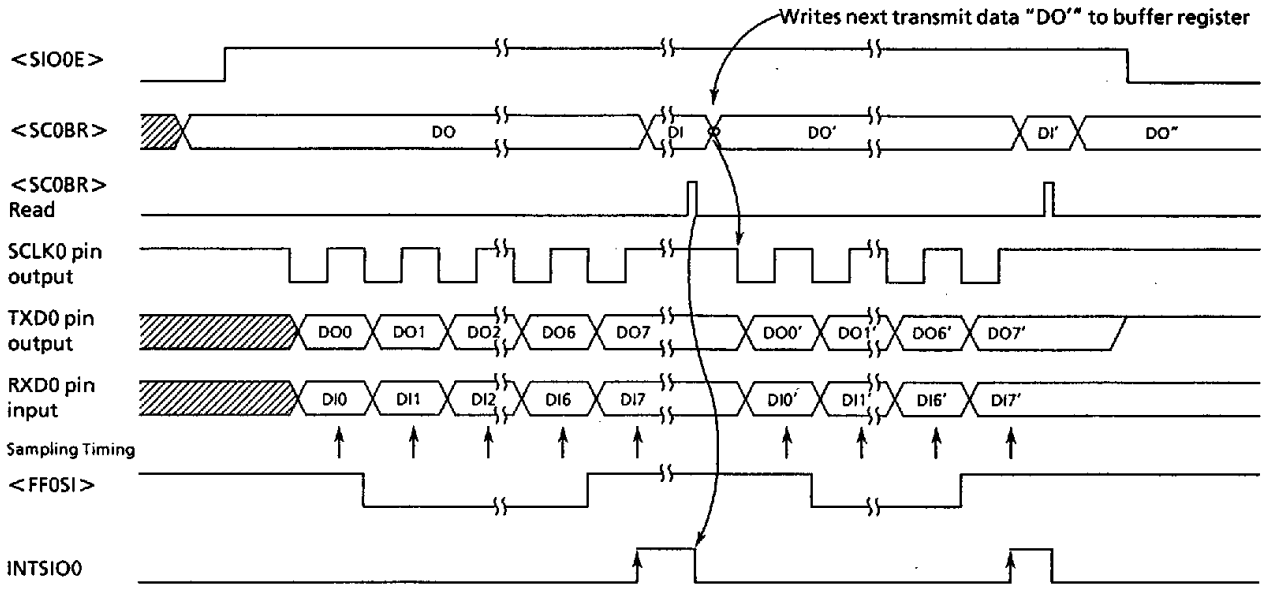
To end the simultaneous transmit-receive operation, clear the serial transfer register<SIO0E> or <SIO1E> to "0".

When the serial transfer enable/disable register<SIO0E> or <SIO1E> is cleared to "0", the simultaneous transmit-receive operation ends after the 8 bits of receive data are fetched and transferred to the buffer register.

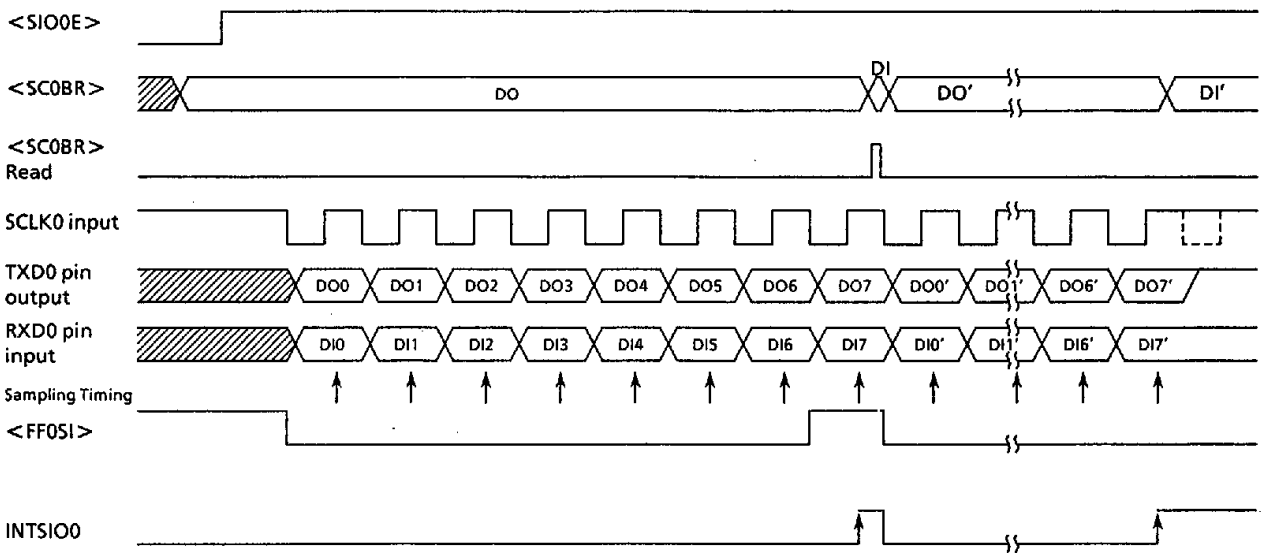
In the simultaneous transmit-receive mode, the serial transfer operation ends just after setting <S0RES> or <S1RES> to "1", and the serial transfer enable/disable register <SIO0E> or <SIO1E> is cleared to "0".

The end of simultaneous transmit-receive can be confirmed by reading the serial transfer monitor flags<FF0SI> or <FF1SI> in program.

An end of the simultaneous transmit/receive operation can be confirmed by reading the serial transfer monitor flag <FF0SI> or <FF1SI> in program.



(a) Internal clock operation in simultaneous transmit/receive mode (with wait)



(b) External clock operation in simultaneous transmit/receive mode

Fig 3.17.7 Serial channel Timing chart in Simulaneous Transmit/Receive mode

3.18 SERIAL BUS INTERFACE (SBI)

TMP90CR74A has one (1) channel serial BUS interface (SBI) on chip, which has two operation modes. One is I2C-BUS and another is 8-bit clock synchronous serial port. The interface terminals for communication are multiplexed and named channel 0 and 1. These sets of terminals can be switched by software. (I2C-BUS is the BUS system proposed by Philips.)

In I2C-Bus mode, the interface terminals can be selected from two (2) channels.

- Channel 0 ; P52 (SDA0), P53 (SCL0)
- Channel 1 ; P55 (SDA1), P56 (SCL1)

In SIO mode, the interface terminals can use only channel 0.

- Channel 0 ; P52 (RXD2), P53 (SCLK2), P54 (TXD2)

The terminals for I2C-BUS are multiplexed with P5 port and these are used as normal port when not to use as I2C-BUS. In order to use these port as I2C-BUS, the output latch of port should be set "1" and output mode when the terminal needs to be used as output or I/O in I2C-BUS mode. For the terminal of RxD2, the I/O mode should be set as input mode.

I2C-Bus Function

- Master / Slave Switching
- Single Master System without BUS arbitration
- High Speed Capability with 8-level FIFO in Master mode
- 9-bit data (8-bit data and 1-bit acknowledge)

SIO Functions

- 8-bit data Transfer Synchronizing with Serial Clock
- Transmission mode / Transmit-receive mode / Receive mode
- 1-byte Transfer

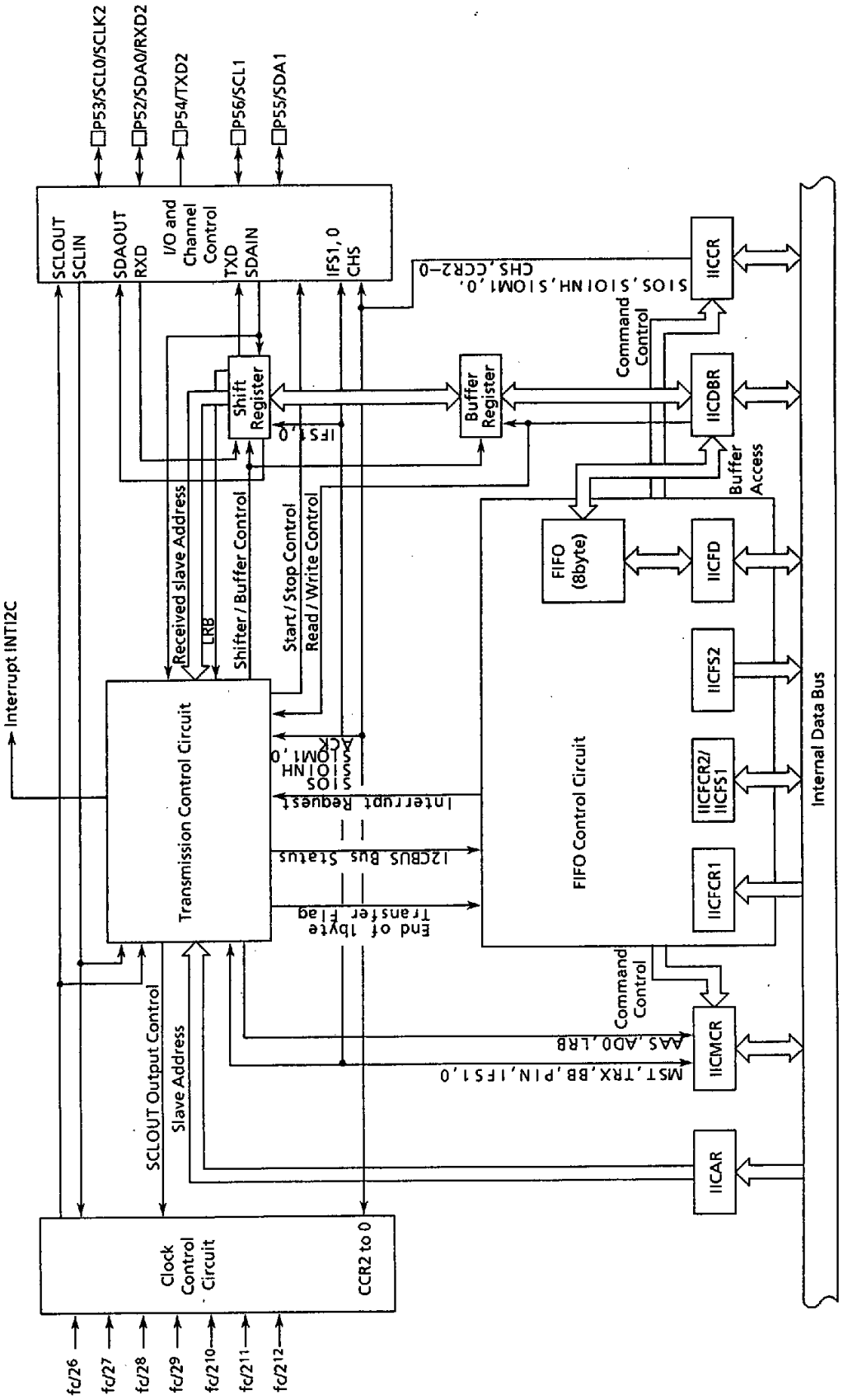


Fig 3.18.1 Configuration of Serial BUS Interface

3.18.1 Control

The following control registers can be used to control and monitor the Serial BUS interface circuit in I2C-BUS mode.

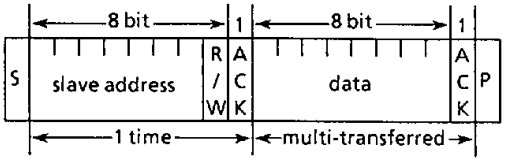
- Serial BUS Interface Control Register 1 (SBICR1)
- Serial BUS Interface Control Register 2 (SBICR2)
- Serial BUS Interface Data Buffer Register (SBIDBR)
- I2C-BUS Address Register (I2CAR)
- Serial BUS Interface Status Register (SBISR)

The function of the above registers are different in each operation mode.

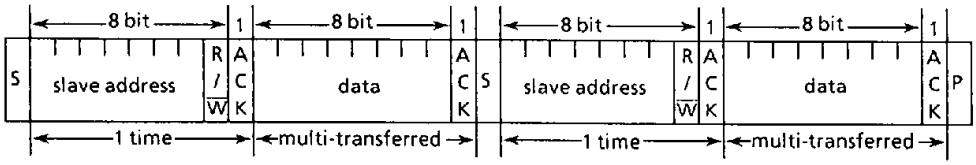
3.18.2 Data Format in I2C-BUS mode

The followings shows the data format in I2C-BUS mode.

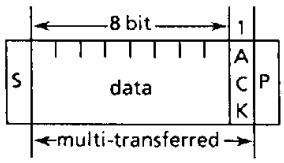
(a) Addressing format : transferring between master and addressed slave



(b) Addressing format (restart) : in case the direction for transferring is changed



(c) Free data format : transferring format for data only; transferring neither involving slave address nor R/$\overline{W}$ bit



Note
S : start condition : Output timing pulse which indicates start transmitting.
R/$\overline{W}$: direction bit : Indicate the direction for transferring against slave.
0 : slave receives (master transfers)
1 : slave transfers (master receives)
ACK : acknowledge bit : Receiver response to transmitting as a confirmation for data receiving
0 : receiving completed
1 : not accepting data transferred, or in case master receiver instructs slave transmitter to terminate transferring.
P : stop condition : Output timing pulse which indicates terminate transmitting

Fig 3.18.2 Data Format for I2C-BUS Mode

3.18.3 Control in I²C-BUS mode.

The following registers are used to control and monitor the serial BUS interface in I²C-BUS mode.

Serial BUS Interface Control Register 1

SBICR1 (FFE2H)

7	6	5	4	3	2	1	0
"0"	"0"	"0"	ACK	CHS		SCK	

(Reset Value 0000 0000)

ACK	Acknowledge bit select	0 : Acknowledge not returned to transmitter. 1 : Acknowledge returned to transmitter.	R/W
CHS	Input / Output channel select	0 : Channel 0 (SCL0, SDA0) 1 : Channel 1 (SCL1, SDA1)	
SCK	Serial clock frequency select (available in master mode)	000 : fc/2⁶ (250 kHz) 001 : fc/2⁷ (125 kHz) 010 : fc/2⁸ (62.5 kHz) 011 : fc/2⁹ (31.2 kHz) 100 : fc/2¹⁰ (15.6 kHz) 101 : fc/2¹¹ (7.8 kHz) 110 : fc/2¹² (3.9 kHz) 111 : — at fc = 16 [MHz]	write only

Note : Always writing "0" in 5, 6, 7bits of SBICR1.

Serial BUS Interface Data Buffer Register

SBIDBR (FFE3H)

7	6	5	4	3	2	1	0

(R/W)

I²C-BUS Address Register

I2CAR (FFE4H)

7	6	5	4	3	2	1	0
SA6	SA5	SA4	SA3	SA2	SA1	SA0	ALS

(Reset Value 0000 0000)

ALS	Address confirm	0 : Confirm slave address (addressing format) 1 : Not confirm slave address (free data format)	write only

Serial BUS Interface Control Register 2

SBICR2 (FFE5H)

7	6	5	4	3	2	1	0
MST	TRX	BB	PIN	SBIM		"0"	"0"

(Reset Value 0001 00**)

MST	(Write) Master / slave selection (Read) Status monitoring	0 : Slave 1 : Master	R/W
TRX	(Write) Transmission / Receive selection (Read) Status monitoring	0 : Receiver 1 : Transmitter	
BB	(Write) Start / stop condition control (Read) I²C-BUS status monitor	(Write) 0 : Stop condition generate 1 : Start condition generate (Read) 0 : BUS free 1 : BUS busy	
PIN	(Write) Interrupt request reset (Read) Interrupt request monitor	(Write) 0 : - 1 : Interrupt request reset (Read) 0 : Interrupt request 1 : No request	
SBIM	Serial BUS Interface operating mode selection	00 : Port mode 01 : SIO mode 10 : I²C-BUS mode 11 : reserved	Write only

Serial BUS Interface Status Register

SBISR (FFE5H)

7	6	5	4	3	2	1	0
					AAS	AD0	LRB

(Reset Value **** ****)

AAS	Slave address match detection monitor	0 : – 1 : Slave addr match or general call detect	read only
AD0	General Call detection monitor	0 : – 1 : General Call detect	
LRB	Last receive bit monitor (Acknowledge monitor)	0 : Last receive bit "0" (Acknowledge) 1 : Last receive bit "1" (No-Acknowledge)	

(1) Set the ACK (bit 4 in the SBICR1) to "1" for operation in the acknowledge mode.

In the receive mode during the clock pulse cycle, the SDA pin is set to the low-level in order to generate the acknowledge signal. When the ACK is cleared to "0", the SDA pin released high-level in the acknowledge timing.

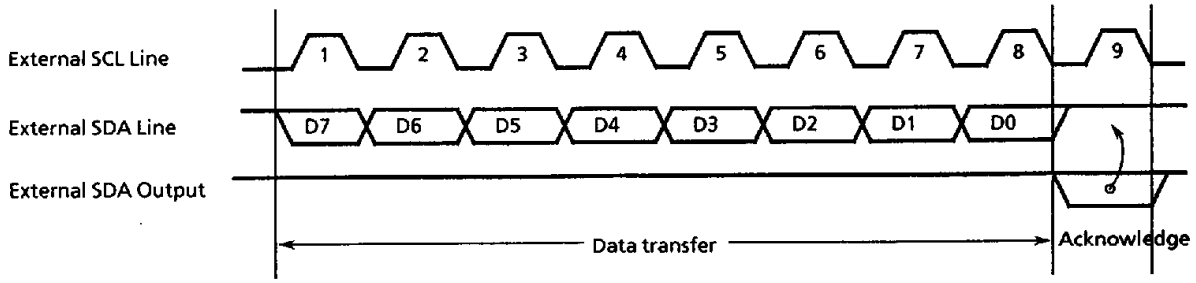


Fig 3.18.3 Acknowledge Signal Output Timing

(2) Input / Output channel setting

The channel can be selected by setting <CHS> bit in SBICR1 register.

Channel 1 (pair of SCL1 and SDA1) is selected by setting "1" to <CHS> and Channel 0 (pair of SCL0 and SDA0) is selected by setting "0" to <CHS>.

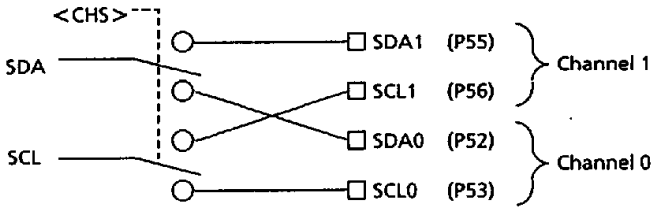


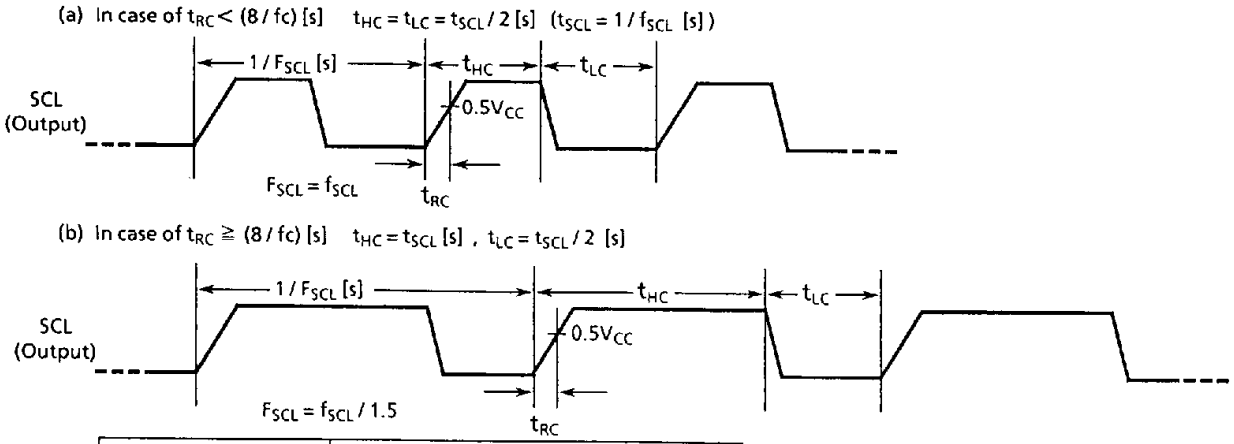
Fig 3.18.4 Input/Output Channel

(3) Serial Clock

The SCK (bits 2 to 0 in the SBICR1) is used to select a maximum transfer frequency directed from the SCL pin in the master mode.When rising time of the output clock (t_{RC}) is at least 8/fc [s], a high-level time of the output clock (t_{HC}) is tSCL.

While the SCL line is fixed to low-level by a slave device,the output clock stops.

The first clock (t_{HC} [s]) after restart is ($t_{SCL}/2$) $\leqq t_{HC} \leqq t_{SCL}$.



SCK (Bit 2 to 0 of SBICR1)	F_{SCL} (at fc = 16 MHz)	
	t_{RC} < 500 [ns]	500 [ns] ≦ t_{RC}
000	250 kHz	166.7 kHz
001	125 kHz	83.3 kHz
010	62.5 kHz	41.7 kHz
011	31.2 kHz	20.8 kHz
100	15.6 kHz	10.4 kHz
101	7.8 kHz	5.2 kHz
110	3.9 kHz	2.6 kHz
	In case of (a)	In case of (b)

Fig 3.18.5 Serial Clock

(4) Slave Address and Address Recognize mode

To use 90CR74A as a slave device, set the slave address <SA6 to 0> and <ALS> to I2CAR register. Set <ALS> "0" to the for the address recognition mode.

(5) Master / Slave Selection

Set the MST (bit 7 in the SBICR2) to "1" for operating the 90CR74A as a master device. The MST is cleared to "0" by the handware after a stop condition on the bus is detected.

(6) Transmitter / Receiver Selection

Set the TRX (bit 6 in the SBICR2) to "1" for operating the 90CR74A as a transmitter. Reset the TRX for operation as a reciver. When 90CR74A receives a slave address setted in I2CAR or a GENERAL CALL from the master device in the addressing format is transferred in the slave mode, the TRX is set to "1" if the direction bit (R/W) sent from the master device is "1", and is cleared to "0" if the bit is "0".

In the master mode, after an acknowledge signal is returned from the slave device, the TRX is set to "0" if a transmitted direction bit is "1", and set to "1" if it is "0".

When an acknowledge signal is not returned, the current condition is maintained.

The TRX is cleared to "0" by the hardware after a stop condition on the I2C bus is detected.

(7) Start / Stop Condition Generation (for Master Mode)

A start condition and 8-bit of data (a slave address and a direction bit which are set to a data buffer register) are output on a bus by writing "1" to the MST, TRX, and BB when the BB (bit 5 in the SBICR2) is "0".

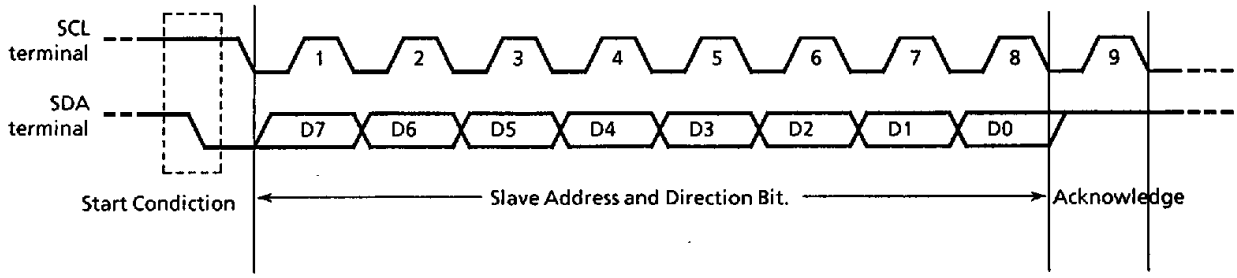


Fig 3.18.6 Start Condition and Slave Address Generation

When the BB is "1", a sequence of generating a shop condition is started by writing "1" to the MST, TRX, and PIN, and "0" to the BB. Do not modify the contents of MST, TRX, BB, and PIN until a shop condition is generated on a bus.

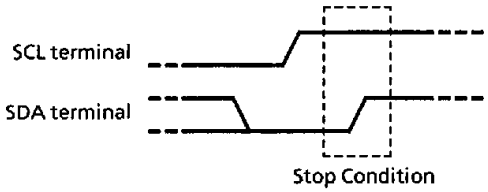


Fig 3.18.7 Stop Condition Generation

The BUS condition can be monitored by check <BB> bit in SBISR register. The <BB> bit is set "1" when start condition is detected on SCL and SDA and is set "0" when stop condition is detected on the BUS.

(8) Cancel interrupt service request

When a serial bus interface interrupt request (INTSBI) occurs, the PIN (bit 4 in the SBISR) is cleared to "0". During the time that the PIN is "0", the SCL pin is pulled down to the low level.
The PIN is cleared to "0" when 1-byte of data is transmitted or received. Either writing/reading data to/from the SBIDBR sets the PIN to "1".
The time from the PIN being set to "1" until the SCL pin is released takes tLOW.
In the address recognition mode (ALS = 0), the PIN is cleared to "0" when the received slave address is the same as the value set to the I2CAR or when a GENERAL CALL is received (all 8-bit data are "0" after a start condition). Although the PIN (bit 4 in the SBICR2) can be set to "1" by the program, the PIN is not cleared to "0" when it is written "0".

(9) Serial bus interface operation mode selection

The SBIM (bits 3, 2 in the SBICR2) is used to specify the serial bus interface operation mode. Set the SBIM to "10" when used in the I2C bus mode after confirming that input signal via port is high level. Switch a mode to port after confirming sure that the bus is free.

(10) Slave address match detection monitor

The AAS (bit 2 in the SBISR) is set to "1" in the slave mode, in the address recognition mode (ALS = 0), or when receiving GENERAL CALL or a slave address with the same value that is set to the I2CAR. When the ALS is "1", the AAS is set to "1" after receiving the first 1-byte of data. The AAS is cleared to "0" by writing/reading data to/from a data buffer register.

(11) GENERAL CALL detection monitor

The AD0 (bit 1 in the SBISR) is set to "1" in the slave mode, when all 8-bit data received after a start condition are "0". The AD0 is cleared to "0" when a start or stop condition is detected on a bus.

(12) Last received bit monitor

The SDA line value stored at the rising edge of the SCL line is sent to the LRB (bit 0 in the SBISR). In the acknowledge mode, immediately after an INTSBI interrupt request is generated an acknowledge signal is read by reading contents of the LRB.

2.18.4 Data Transfer in I2C bus Mode

(1) Set the ACK, CHS and SCK in the SBICR1. Specify "0" to bits 7 to 5.
Set a slave address and the ALS (ALS = 0 when an addressing format) to the I2CAR.
After confirming that input signals via port are high level, for specifying the default setting to slave receiver mode, assign "0" to the MST, TRX, and BB in the SBICR2; "1" to the PIN; "10" to the SBIM; and "0" to bits 0 and 1.

(2) Confirm a bus free status (When BB = 0).
Set the ACK to "1" and specify a slave address and a direction bit to be transmitted to the SBIDBR. When the BB is "0", the start condition are generated and the slave address and the direction bit which are set to the SBIDBR are output on a bus by writing "1" to the MST, TRX, BB, and PIN. A slave device receive these data and pulls down the SDA line of a bus to the low-level at the acknowledge signal timing. An INTSBI interrupt request occurs at the 9th falling edge of the SCL clock cycle, and the PIN is cleared to "0".
The SCL pin is pulled down to the low-level while the PIN is "0". When an interrupt request occurs, the TRX changes by the handware according to the direction bit only when an acknowledge signal is returned from the slave device.

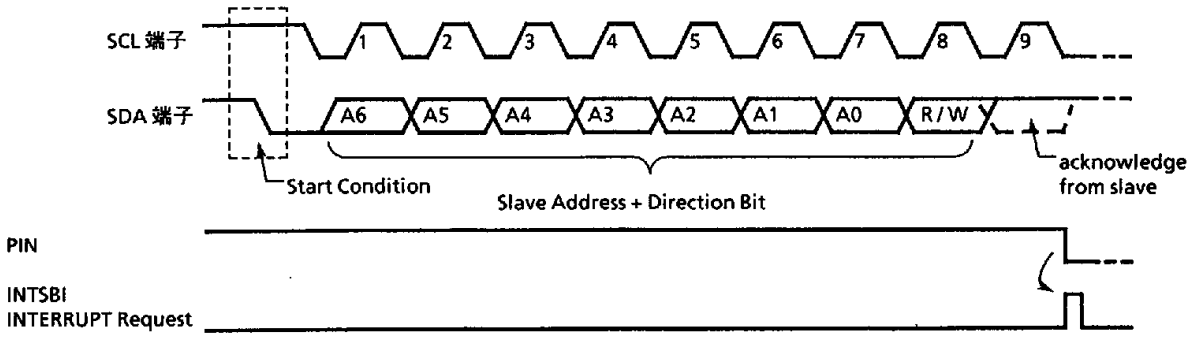


Fig 3.18.8 Start Condition and Slave Address Generation

(3) 1-byte Data Transfer
Test the MST by the INTSBI interrupt process after a 1-byte data transfer is completed, and determine whether the mode is a master or slave.

a. When the MST is "1" (Master mode)
Check the TRX and determine whether the mode is a transmitter or receiver.

① When the TRX is "1" (Transmitter mode)
Check the LRB. When the LRB is "1", a receiver does not request data. Implement the process to generate a stop condition (described later) and terminate data transfer.
When the LRB is "0", the receiver requests new data. Write the transmitted data to the SBIDBR. After writing the data, the PIN becomes "1", a serial clock pulse is generated for transferring a new 1-byte of data from the SCL pin, and then the 1-byte data is transmitted from SDA pin. After the data is transmitted, an INTSBI interrupt request occurs. The PIN becomes "0" and the SCL pin is pulled down to the low level. If the data to be transferred is more than one word in length, repeat the procedure from the LRB checking above.

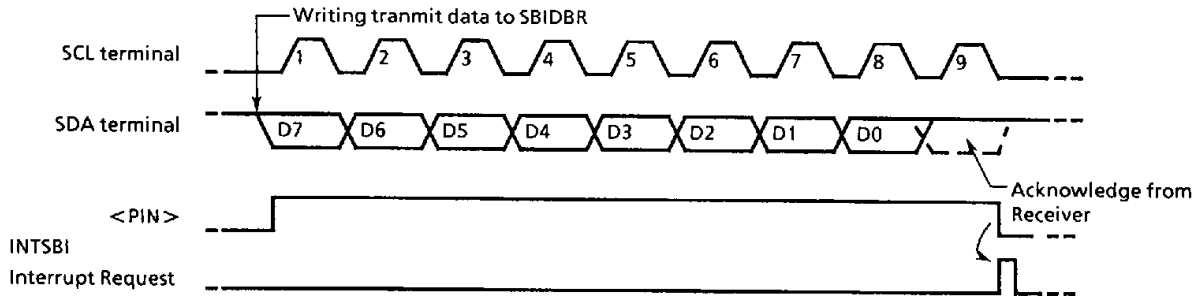


Fig 3.18.9 1-byte Transmission

② When the TRX is "0" (Receiver mode)

Set the ACK to "1" and read the received data from the SBIDBR (data which is read immediately after a slave address is sent is undefined). After the data is read, the PIN becomes "1". The 90CR74A outputs a serial clock pulse to the SCL pin to transfer new 1-byte of data and sets the SDA pin to "0" at the acknowledge signal timing.

An INTSBI interrupt request occurs, the PIN becomes "0" and the SCL pin pulled down to the low level. The 90CR74A outputs a clock pulse for 1-byte of data transfer and the acknowledge signal each time that received data is read from the SBIDBR.

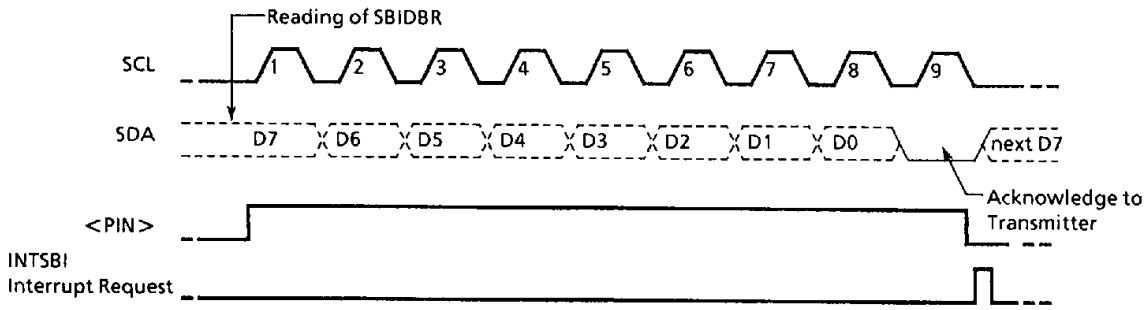


Fig 3.18.10 1-byte Receive

In order to terminate transmitting data to a transmitter, clear the ACK to "0" before reading data which is 1-byte before the last data to be received. The SDA pin released high-level in an acknowledge timing of last received byte. The receiver indicates to the transmitter that data transfer is complete. After data is received and an interrupt request has occurred, the 90CR74A generates a stop condition and terminates data transfer. When reading data from SBIDBR in the last received byte, the serial clock and acknowledge signal don't outputs because ACK is "0".

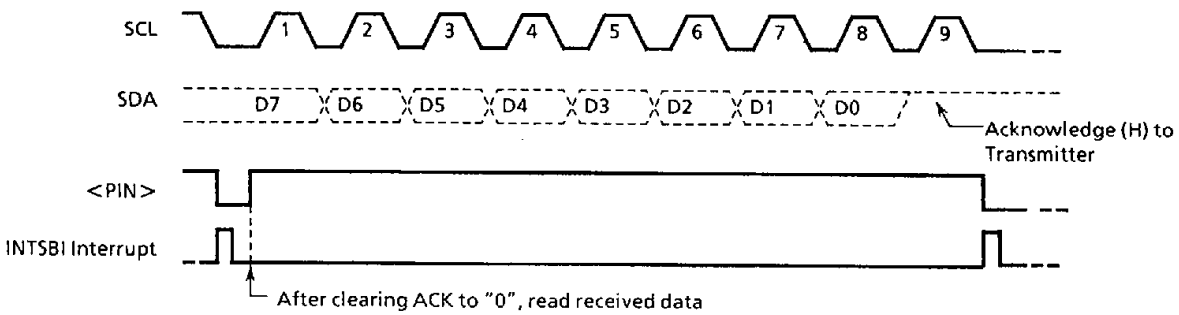


Fig 3.18.11 Data Transmission of Final Data in Master/Receiver mode

b.When the MST is "0" (Slave mode)

In the slave mode, an INTSBI interrupt request occurs when the 90CR74A receives a slave address or a GENERAL CALL from the master device, or when a GENERAL CALL is received and data transfer is complete after matching a received slave address. When an INTSBI interrupt request occurs, the PIN (bit 4 in the SBICR2) is reset, and the SCL pin is pulled down to the low level. Either reading/writing from/to the SBIDBR or setting the PIN to "1" releases the SCL pin after taking tLOW time.

In the slave mode, the 90CR74A operates either in normal slave mode.

The 90CR74A tests the TRX (bit 6 in the SBISR), the AAS (bit 2 in the SBISR), and the AD0 (bit 1 in the SBISR) and implements processes according to conditions listed in the next table.

Table 3.18.1 Status and Service in Slave mode

TRX	AAS	AD0	Status	Service
1	1	0	In Slave / Receiver mode, received the slave address of 90CR74A with direction bit "1". This condition is slave transmit mode by transfer request from master device.	Write transmit data into SBIDBR register.
	0	0	In Slave / Transmitter mode, 1-byte transmission has completed.	In case of <LRB> = "1" (no further data request), set <PIN> "1" and <TRX> "0" for BUS release. In case of <LRB> = "0" (further data request), write transmit data to SBIDBR register.
0	1	1/0	In Slave / Receiver mode, received address of 90CR74A with direction bit "0" or General Call. This condition is slave receive mode by receive request from master device.	Read SBIDBR register in order to set <PIN> "1" (dummy read).
	0	1/0	In Slave / Receiver mode, 1-byte receive has completed.	Read received data from SBIDBR register.

(4) When the BB is "1", a sequence of generating a stop condition is started by writing "1" to the MST, TRX, and PIN, and "0" to the BB. Do not modify the contents of the MST, TRX, BB, PIN untila stop condition is generated a bus.

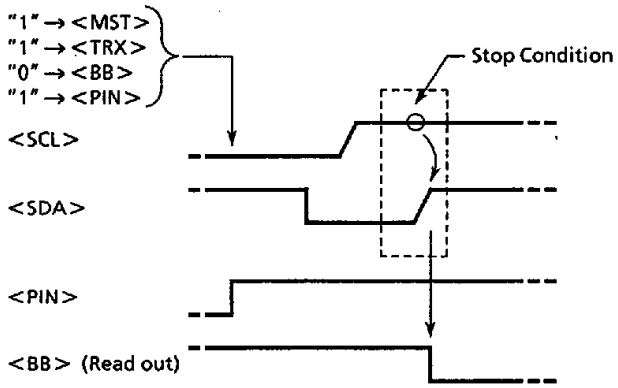


Fig 3.18.12 Stop Condition Generation

(5) Restart

Restart is used to change the direction of data transfer between a master device and a slave device during transferring data. The following explains how to restart when the 90CR74A is in the master mode.

Specify "0" to the MST, TRX, and BB and "1" to the PIN and release the bus. The SDA pin retains the high level and the SCL pin is released. Since a stop condition is not generated on the bus, the bus is assumed to be in a busy state from other devices. Test the BB until it becomes "1" to check that the SCL pin of the 90CR74A is released. Test the LRB until it becomes "1" to check that the SCL line of the bus is not pulled down to the low level by other devices. After confirming that the bus stays in a free state, generate a start condition with procedure (2).

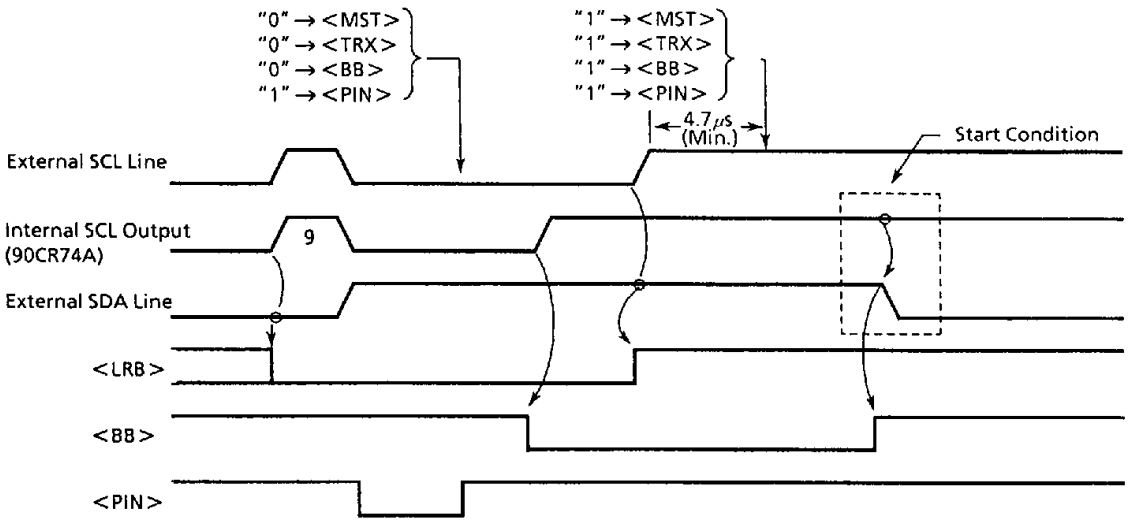


Fig 3.18.13 TMP90CR74A Restart Timing Chart

3.18.5 FIFO Controling

In I2C-BUS / Master mode, 8-byte continuous data transfer can be done with FIFO control.

I2C-BUS control registers are accessed from FIFO control circuit instead of CPU. Before starting FIFO control circuit, I2C-BUS should be set in slave mode (initialized condition). FIFO control circuit is controlled by following registers,

I2C-BUS FIFO Control Register 1

I2CFCR1 (FFE6H)

7	6	5	4	3	2	1	0
T/$\overline{R}$	FSCK			CONT	BYTE		

(Reset Value 0000 0000)

T/$\overline{R}$	FIFO transfer mode selection	0 : Receiver mode 1 : Transmitter mode	Write only
FSCK	Serial clock frequency (fscl) selection	000 : fc/2^6 (250 kHz) 001 : fc/2^7 (125 kHz) 010 : fc/2^8 (62.5 kHz) 011 : fc/2^9 (31.2 kHz) 100 : fc/2^{10} (15.6 kHz) 101 : fc/2^{11} (7.8 kHz) 110 : fc/2^{12} (3.9 kHz) 111 : — at fc = 16 [MHz]	
CONT	Data transfer mode selection	0 : 8-byte data transfer 1 : Continuous transfer	
BYTE	Number of transfer data byte (Data is valid when <CONT> = "0")	000 : 1-byte 001 : 2-byte 010 : 3-byte 011 : 4-byte 100 : 5-byte 101 : 6-byte 110 : 7-byte 111 : 8-byte	

I2C-BUS FIFO Control Register 2

I2CFCR2 (FFE7H)

7	6	5	4	3	2	1	0
$\overline{START}$	$\overline{STOP}$	CHS	$\overline{INT}$			$\overline{RST}$	

(Reset Value 1101 **1*)

$\overline{START}$	Start FIFO buffer transfer	0 : Start or restart 1 : –	Write only
$\overline{STOP}$	Stop FIFO buffer transfer	0 : Stop 1 : –	
CHS	Input / Output Channel selection	0 : Channel 0 (SCL0, SDA0) 1 : Channel 1 (SCL1, SDA1)	
$\overline{INT}$	Restart in continuous mode	0 : Start continuous transfer 1 : –	
$\overline{RST}$	Reset for I2C-BUS and FIFO control circuit (Notice)	0 : Reset 1 : –	

Notice : Since 4.5-state width system reset is executed after writing to this register, Do not access with I2CBUS or FIFO controller during the period.

I²C-BUS FIFO Data Buffer Register

I2CFDBR (FFE8H)

7	6	5	4	3	2	1	0
FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

(Reset Value **** ****) (R/W)

I²C-BUS FIFO Status Register 1

I2CFSR1 (FFE7H)

7	6	5	4	3	2	1	0
SDA	END	CHS	BUSY	FULL	EMPTY	SCERR	AKERR

(Reset Value *000 0000)

SDA	SDA line monitor	0 : SDA line low 1 : SDA line high	read only
END	FIFO buffer status flag	1 : End of transfer cleared by setting <STOP> to "0"	
CHS	Input / Output channel monitor	0 : Channel 0 1 : Channel 1	
BUSY	FIFO buffer transfer status	1 : FIFO buffer data in transfer cleared by setting <STOP> to "0"	
FULL	FIFO buffer full / Receive end	0 : – 1 : FIFO buffer full / receive end	
EMPTY	FIFO buffer empty/Transmit end	0 : – 1 : FIFO buffer empty / Transmit end	
SCERR	Start condition error	0 : – 1 : Start condition error	
AKERR	Acknowledge error	0 : – 1 : Acknowledge error	

I²C-BUS FIFO Status Register 2

I2CFSR2 (FFE9H)

7	6	5	4	3	2	1	0
NOMAT	LRBM						

(Reset Value 01** ****)

NOMAT	Matching monitor between SCL line and SCL terminal	0 : – 1 : SCL line pulled down by slave device	read only
LRBM	Last received bit monitor (acknowledge signal monitor)	0 : Last bit "0" (acknowledge) 1 : Last bit "1" (no-acknowledge)	

(1) Transmit Operation

Set the number of byte transferred and select transfer clock by setting I2CFCR1 register. Set FIFO controller in transmitter mode by setting "1" to <T/$\overline{R}$> bit in I2CFCR1 register. The number of byte for transfer at start time includes slave address. This can be set up to 8 bytes. By setting <CONT> bit in I2CFCR1 register, the number of byte is set to 8bytes and continuous data transfer becomes available. After setting I2CFCR1 register, write data into I2CFDBR in order of transmission. When number of data written becomes the number of byte set, <FULL> bit in I2CFSR1 register is set "1". It's ignored if data is written during <FULL> is "1". For starting transmission, slave address and <R/$\overline{W}$> bit should be set as the first data.

Then set <CHS> and <START> bits in I2CFCR2, the FIFO controller becomes active.

The FIFO controller sets <BUSY> bit in I2CFSR "1" and accesses I2CFCR1, I2CFDBR and I2CFCR2 registers to start transmission. At this time, if BUS is busy, <SCERR> bit in I2CFSR register is set "1" and generate the interrupt request INTSBI. If this happens, set <$\overline{RST}$> bit in I2CFCR2 to "1" and reset FIFO controller by software.

If there is no acknowledge return for each byte, the interrupt request INTSBI is generated and <AKERR> bit in I2CFSR register is set "1".

When all data byte has been transferred, <EMPTY> bit in I2CFSR register is set "1" and the interrupt request INTSBI is generated. And if <CONT> bit in I2CFCR1 register is "0", <END> bit in I2CFSR register is set "1" to terminate all data transfer. In case that <CONT> bit is "1", <END> bit is not set because of continuous mode. This is the reason why the rest of data should be transferred by restarting after setting the number of data remained and data into I2CFCR1 and I2CFDBR registers. If an interrupt request is no needed when data transfer completes, set <$\overline{INT}$> to "0" before restart.

(2) Receive Operation

The procedure is almost same as transmit operation except that the number of data byte does not include slave address. Set the FIFO controller in Receiver mode by setting <T/$\overline{R}$> bit in I2CFCR1 register. Following that, set slave address and <R/$\overline{W}$> bit to I2CFDBR register and set FIFO controller active by setting <START> bit in I2CFCR2 to "0". When the number of data, which was set in I2CFCR1 register, has been received, <FULL> bit in I2CFSR register is set "1" and the interrupt request INTSBI is generated. The status can be monitored in <CONT> and <$\overline{INT}$> bits and I2CFSR register as same as in transmit operation.

The content of dummy read, which is executed right after the slave address, is not set into FIFO buffer.

(3) Restart Operation

When <END> bit is "1", to provide the following procedure can be recognized as restart operation,

Start preparation as same as (1) or (2)

Start by setting <$\overline{START}$> bit "0"

The FIFO controller does restart operation then data is transferred.

(4) Stop Operation

By setting I2CFCR2 <$\overline{STOP}$> to "0" when <END> bit in I2CFCR1 register is "1", FIFO controller stops data transfer after generate stop condition on to BUS and clearing <BUSY> bit in I2CFSR1 register is "0".

3.18.6 Control in Clock Synchronous 8-bit SIO mode

To use serial BUS interface as clocked synchronous 8-bit SIO mode, the following registers are used.

Serial BUS Interface Control Register 1

SBICR1 (FFE2H)

7	6	5	4	3	2	1	0
SIOS	SIO INH	SIOM		CHS	SCK		

(Reset Value 0000 *000)

SIOS	Transfer start / stop	0 : Stop 1 : Start	Write only
SIOINH	Terminate data transfer	0 : Continue 1 : Terminate (stop and clear)	
SIOM	Transfer mode select	00 : 8-bit transmitter mode 01 : reserved 10 : 8-bit transmit/receive mode 11 : 8-bit receiver mode	
CHS	Input / Output channel select	0 : Channel 0 (SCLK2, TXD2, RXD2) 1 : Reserved	R/W
SCK	Serial clock frequency select	000 : fc/2^6 (250 kHz) 001 : fc/2^7 (125 kHz) 010 : fc/2^8 (62.5 kHz) 011 : fc/2^9 (31.2 kHz) } at fc = 16 MHz (to SCLK2 output) 100 : fc/2^{10} (15.6 kHz) 101 : fc/2^{11} (7.8 kHz) 110 : fc/2^{12} (3.9 kHz) 111 : External clock (from SCLK2 input)	Write only

Note 1) * ; don't care
Note 2) SIOS should be "0" during transfer mode and serial clock.

Serial BUS Interface Data Buffer Register

SBIDBR (FFE3H)

7	6	5	4	3	2	1	0

(Initial Value **** ****) Read / Write

Serial BUS Interface Control Register 2

SBICR2 (FFE5H)

7	6	5	4	3	2	1	0
Write "0"	Write "0"	Write "0"	Write "1"	SBIM		Write "0"	Write "0"

(Initial Value **** 00**)

SBIM	Serial BUS Interface operation mode	00 : Port mode (to prohibit Serial Bus Interface) 01 : SIO mode 10 : I^2C-BUS mode 11 : reserved	Write only

Note 1) * ; don't care
Note 2) Should be confirm transfer-end to change terminal from SIO to port

Serial BUS Interface Status Register

SBISR (FFE5H)

7	6	5	4	3	2	1	0
				SIOF	SEF		

(Initial Value **** 00**)

SIOF	Serial transfer operation status	0 : Complete transfer 1 : During transfer	Read only
SEF	Last bit receive monitor (Acknowledge monitor)	0 : Complete data shift 1 : During data shift	

(1) Serial Clock

a. Clock Source

Clock source can be selected by SCK bits in SBICR1 register as follows,

① Internal Clock

In an internal clock mode, any of seven frequencies can be selected. The serial clock is output to the outside on the SCLK2 pin. The SCLK2 pin becomes a high level when data transfer starts. When writing (in the transmit mode) or reading (in the receive mode) data cannot follow the serial clock rate, an automatic-wait function is executed to stop the serial clock automatically and hold the next shift operation until reading or writing is complete.

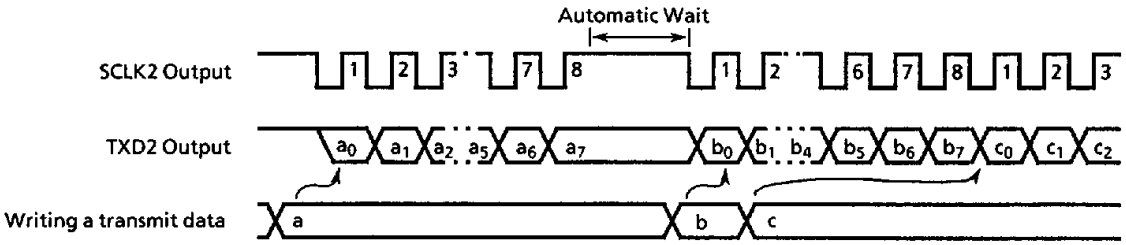


Fig 3.18.14 Automatic Wait Function Timing

② External clock (SCK = "111")

An external clock supplied to the SCLK2 pin is used as the serial clock. In advance, set P53 to input mode. In order to ensure shift operation, a pulse width of longer than 16/fc cyles is required for both high and low levels in the serial clock. The maximum data transfer frequency is 500 kHz (when fc = 16 MHz).

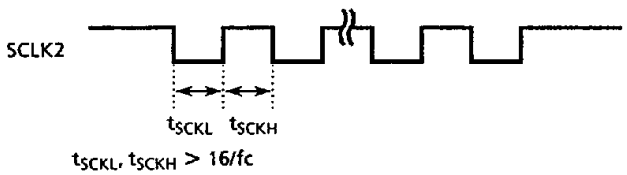


Fig 3.18.15 Maximum Frequency of External Clock

b. Shift Edge

The leading edge is used to transmit data, and the trailing edge is used to receive data.

① Leading edge

The shift timing is the falling edge of the signal at P53 (SCLK2).

② Trailing edge

The shift timing is the rising edge of the signal at P53 (SCLK2).

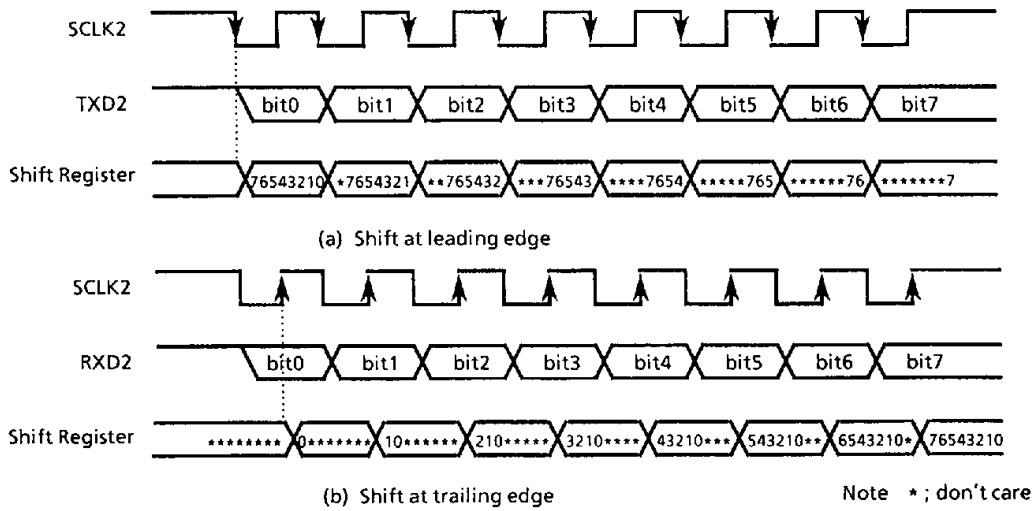


Fig 3.18.16 Shift Edge

(2) Transfer Mode

The SIOM (bits 5 and 4 in the SIO1CR) is used to select a transmit, receive, or transmit/receive mode.

a. 8-bit transmit mode

Set a control register to a transmit mode and write data to the SBIDBR.

After the data is written, set the SIOS to "1" to start data transfer. The transmitted data is transferred from the SBIDBR to the shift register and output to the TXD2 pin in synchronous with the serial clock, starting from the least significant bit (LSB). When the data is transferred to the shift register, the SBIDBR becomes empty. The INTSBI (buffer empty) interrupt request is generated to request new data.

When the internal clock is used, the serial clock will stop and automatic-wait function will be initiated if new data is not loaded to the data buffer register after the specified 8-bit data is transmitted. When new data is written, automatic-wait function is canceled.

When the external clock is used, data should be written to the SBIDBR before new data is shifted. The transfer speed is determined by the maximum delay time between the time when an interrupt request is generated and the time when data is written to the SBIDBR by the interrupt service program.

Transmitting data is ended by clearing the SIOS to "0" by the buffer empty interrupt service program or setting the SIOINH to "1". When the SIOS is cleared, the transmitted mode ends when all data is output. In order to confirm if data is surely transmitted by the program, set the SIOF (bit 3 in the SBISR) to be sensed. The SIOF is cleared to "0" when transmitting is complete. When the SIOINH is set, transmitting data stops. The SIOF turns "0".

When the external clock is used, it is also necessary to clear the SIOS to "0" before new data is shifted; otherwise, dummy data is transmitted and operation ends.

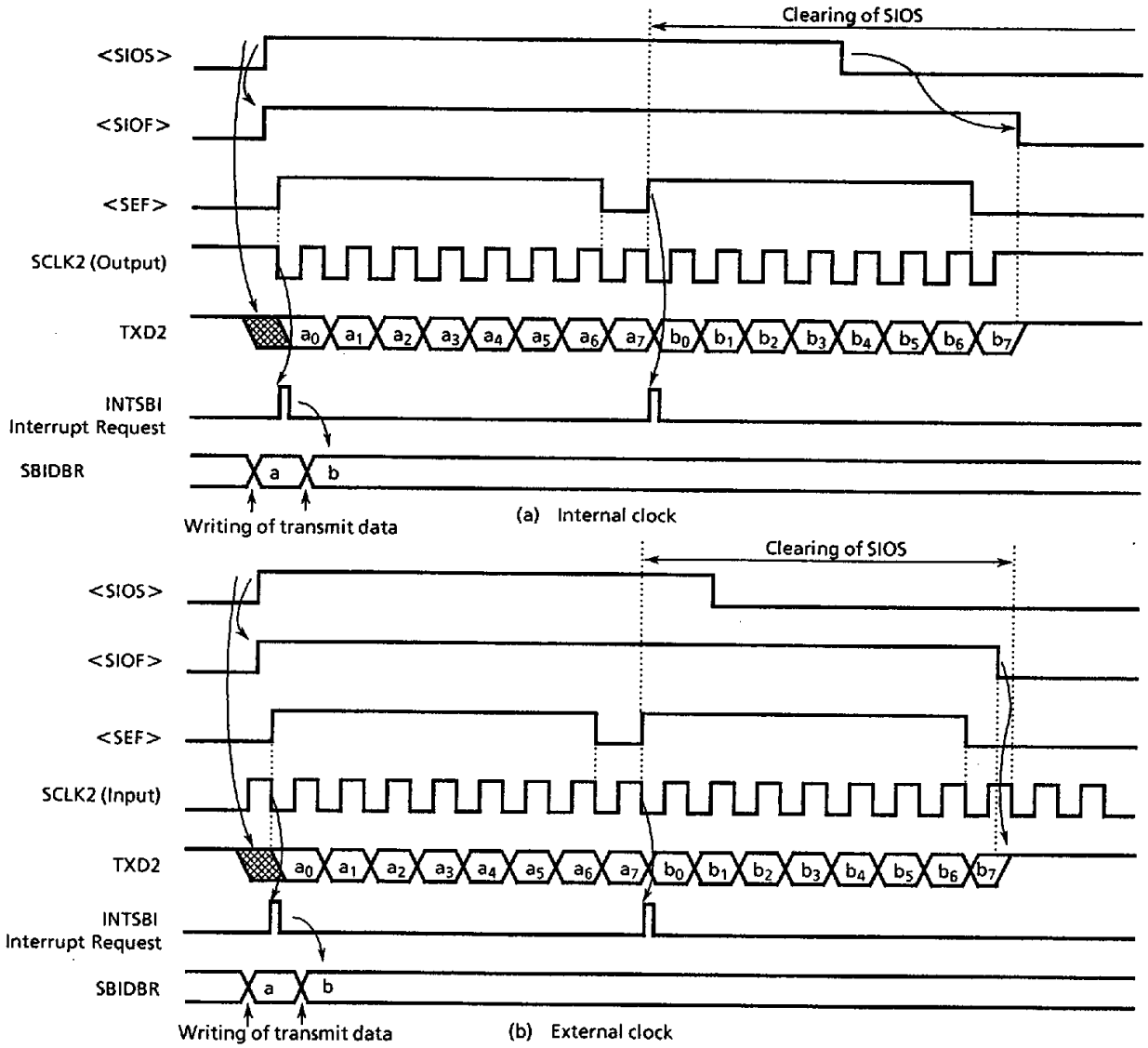


Fig 3.18.17 Transmitter Mode

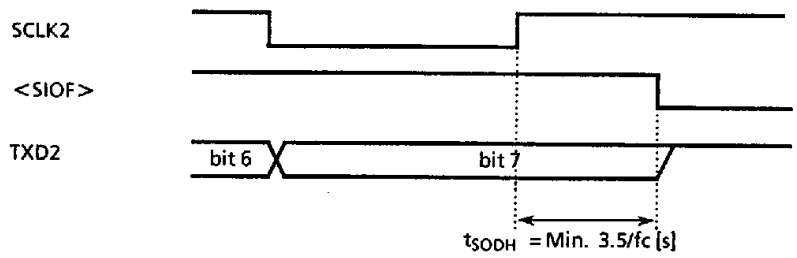


Fig 3.18.18 Data Hold time after Transmission

b. 8-bit Receive Mode

Set a control register to a receive mode and the SIOS to "1" for switching to a receive mode. Data is received from the RXD2 pin to the shift register in synchronous with the serial clock, starting from the least significant bit (LSB). When the 8-bit data is received, the data is transferred from the shift register to the SBIDBR. The INTSBI (buffer full) interrupt request is generated to request of reading the received data. The data is then read from the SBIDBR by the interrupt service program.

When the internal clock is used, the serial clock will stop and automatic-wait function will be initiated until the received data is read from the SBIDBR.

When the external clock is used, since shift operation is synchronized with the clock pulse provided externally, the received data should be read before new data is transferred to the SBIDBR. If the received data is not read, further data to be received is canceled. The maximum transfer speed when the external clock is used is determined by the delay time between the time when an interrupt request is generated and the time when received data is read.

Receiving data is ended by clearing the SIOS to "0" by the buffer full interrupt service program or setting the SIOINH to "1". When the SIOS is cleared, received data is transferred to the SBIDBR in complete blocks. The received mode ends when the transfer is complete. In order to confirm if data is surely received by the program, set the SIOF (bit 3 in the SBIDBR) to be sensed. The SIOF is cleared to "0" when receiving is complete. After confirming that receiving has ended, the last data is read. When the SIOINH is set, receiving data stops. The SIOF turns "0" (the received data becomes invalid, therefore no need to read it).

Note : When the transfer mode is switched, the SBIDBR contents are lost. In case that the mode needs to be switched, conclude receiving data by clearing the SIOS to "0", read the last data, and then switch the mode.

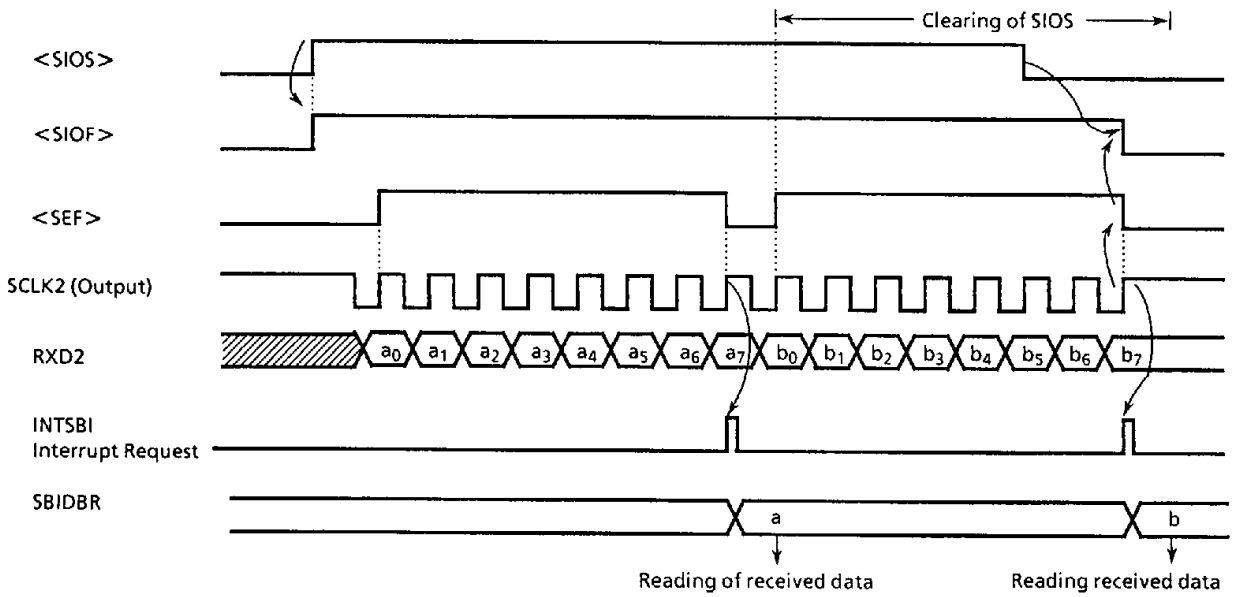


Fig 3.18.19 Data Receive Mode (Internal Clock mode)

c. 8-bit Transmit/Receive Mode

Set a control register to a transmit/receive mode and write data to the SBIDBR. After the data is written, set the SIOS to "1" to start transmitting/receiving. When transmitting, the data is output from the SO pin on the leading edges in synchronous with the serial clock, starting from the least significant bit (LSB). When receiving, the data is input to the SI pin on the trailing edges of the serial clock. 8-bit data is transferred from the shift register to the SBIDBR, and the INTSBI interrupt request occurs. The interrupt service program reads the received data from the data buffer register and writes data to be transmitted. The SBIDBR is used for both transmitting and receiving. Transmitted data should always be written after received data is read.

When the internal clock is used, automatic-wait function is initiated until received data is read and next data is written.

When the external clock is used, since the shift operation is synchronized with the external clock, received data is read and transmitted data is written before new shift operation is executed. The maximum transfer speed when the external clock is used is determined by the delay time between the time when an interrupt request is generated and the time when received data is read and transmitted data is written.

Transmitting/receiving data is ended by clearing the SIOS to "0" by the INTSBI interrupt service program or setting the SIOINH to "1". When the SIOS is cleared, received data is transferred to the SBIDBR in complete blocks. The transmit/receive mode ends when the transfer is complete. In order to confirm if data is surely transmitted/received by the program, set the SIOF (bit3 in the SBISR) to be sensed. The SIOF becomes "0" after transmitting/receiving is complete. When the SIOINH is set, transmitting/receiving data stops. The SIOF turns "0".

Note : When the transfer mode is switched, the SBIDBR contents are lost. In case that the mode needs to be switched, conclude transmitting/receiving data byclearing the SIOS to "0", read the last data, and then switch the transfer mode.

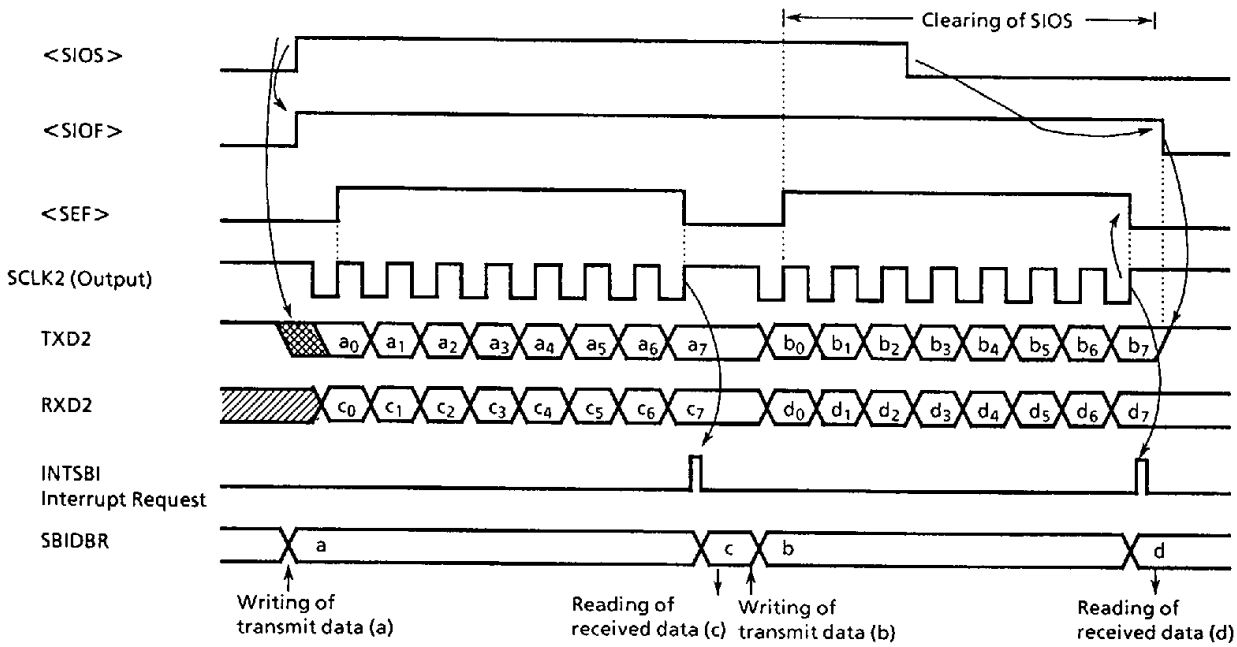


Fig 3.18.20 Transmit/Receive Mode (Internal Clock mode)

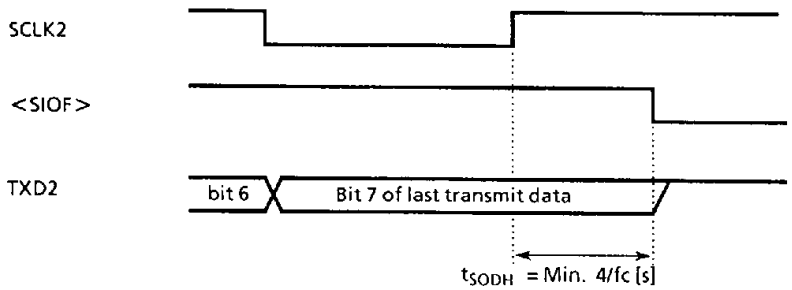


Fig 3.18.21 Data Hold time at End of Transfer (Transmit/Receive mode)

3.19 8-BIT A/D CONVERSION CIRCUIT (A/D)

The TMP90CR74A has an 8-bit A/D conversion circuit of high precision, the successive comparison type with 12-channels analog input. The 10-cannels (AIN0 to AIN9) of 12-channels analog input pin are also used as general purpose input ports (P60 to P67 and P70 to P71). The 2-channels input pin (PDP and PDM) can also be used as the peak hold monitor port of CTL amplifier.

The A/D conversion ends in 11.9 μs (at 16 MHz) from the start of conversion.

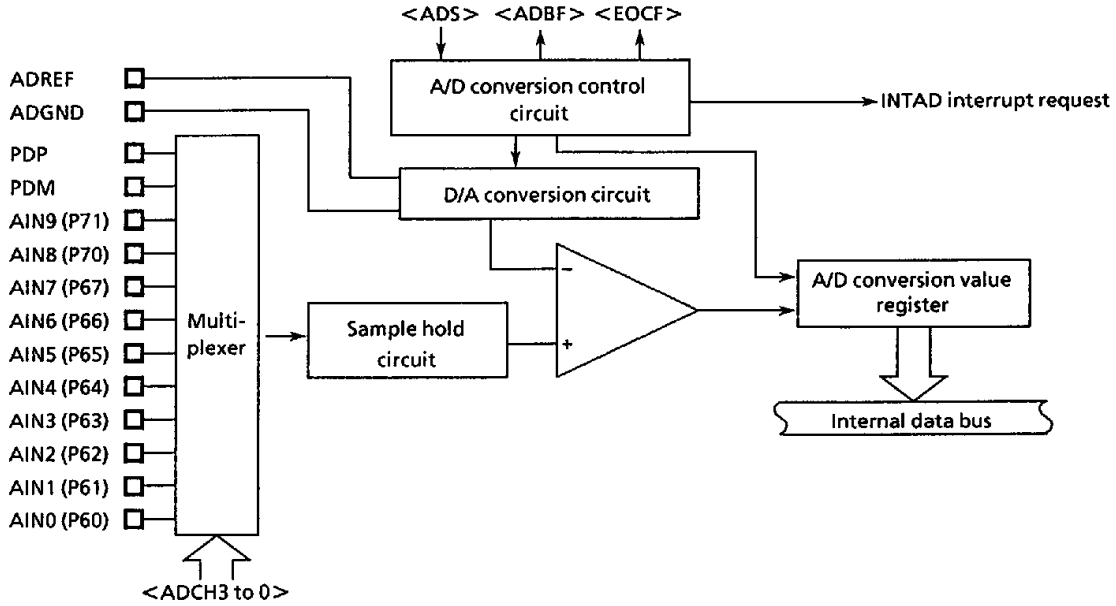


Fig.3.19.1 Configuration of 8-bit A/D Conversion Circuit

3.19.1 Operation of A/D Conversion Circuit

(1) A/D conversion reference voltage

The positive electrode of A/D conversion reference voltage connects to ADREF pin, and the negative electrode of A/D conversion reference voltage connects to ADGND pin.

Apply positive of analog reference voltage to the ADREF pin and negative to the ADGND pin. The A/D conversion is carried out by splitting reference voltage between ADREG pin and ADGND pin to bit divided by 256 by ladder resister and making a judgment by comparing it with analog input voltage.

(2) Analog input channels

One of the 12-channels analog input (AIN0 to AIN9, PDP, PDM) is selected by the A/D conversion control register ADCR<ADCH3-0>.

The analog input channel selection register ADCR<ADCH3 to 0> are initialized to "0, 0, 0" by reset operation, then the AIN0 (P60) is selected. When these ports are not used as the analog input ports, these ports can be used as general purpose input ports (Port6, Port7).

(3) A/D conversion time

The result of A/D conversion is stored into the A/D conversion value register (ADREG) after the passage of 95states from setting the A/D conversion start register ADCR<ADS> to "1".

(4) Start A/D conversion start

A/D conversion is started by setting the A/D conversion control register ADCR<ADS> to "1". After A/D conversion starts, the A/D conversion busy flag ADCR<ADBF> is set to "1".

Note : If A/D conversion is restarted when <ADBF> is "1", A/D conversion is afraid stopped, after confirming <ADBF> to "0".

(5) A/D conversion end

After A/D conversion ends, the A/D conversion end flag ADCR<EOCF> which indicates the end of A/D conversion is set to "1", and the interrupt request signal (INTAD) is generated, and the <ADBF> is cleared to "0".

(6) A/D conversion interruption (INTAD)

After A/D conversion ends, the interrupt request signal (INTAD) is generated, and the A/D circuit requests CPU to interrupt. The interrupt request signal (INTAD) is cleared to "0" by reading out the ADREG in program.

Note: The vecter address of the A/D conversion interrupt (INTAD) is the same as the one of the Timer/Counter3 interrupt (INTT3). The selection of either INTAD or INTT3 can be selected by setting the interrupu control register INTCR<T3ADS>.

(7) Reading of A/D conversion values

The results of A/D conversion is put into the A/D conversion value register (ADREG).
The A/D conversion end flag ADCR<EOCF> is cleared to "0" by reading the ADREG.
The value of the ADREG is an undefined data if the ADREG is read durring A/D conversion.
Figure3.19.2 shows the timing chart of A/D conversion operation.

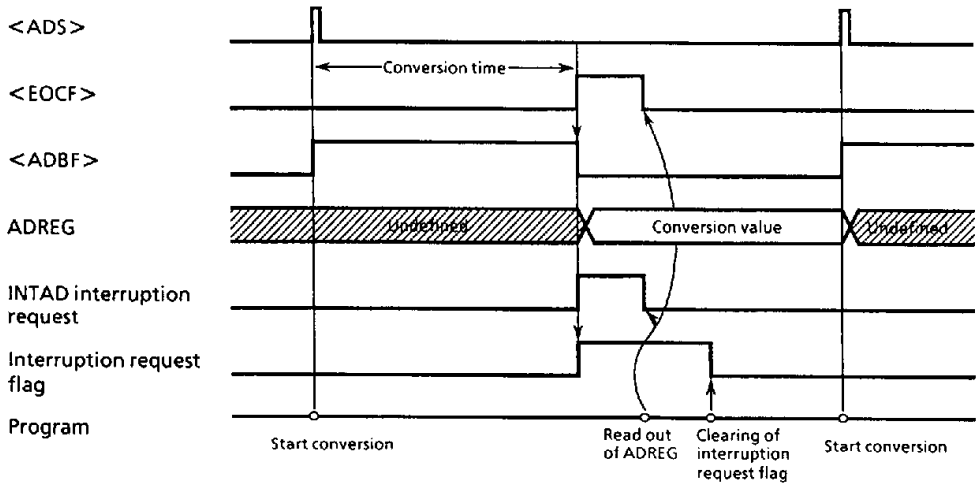


Fig 3.19.2 shown in timingchart of A/D conversion operation.

Note) Executing the HALT instruction during A/D conversion that conversion operation is forced stop, and result in undefined ADREG value.

At the same time, A/D control register is initialized to initial value.

3.19.2 Control Register

A/D conversion control register

ADCR (FFDCH)

7	6	5	4	3	2	1	0
"1"	EOCF	ADBF	ADS	ADCH3	ADCH2	ADCH1	ADCH0

(Initial value 1000 0000)

EOCF	A/D conversion completed flag	0 : A/D conversion in progress or prior to A/D conversion 1 : A/D conversion completed	read only
ADBF	A/D conversion busy flag	0 : A/D conversion stopped 1 : A/D conversion in progress	
ADS	A/D conversion start	0 : – 1 : A/D conversion start (one-shot)	R/W
ADCH3 ADCH2 ADCH1 ADCH0	Analog input channel selection	0000 : Select AIN0 1000 : Select AIN8 0001 : Select AIN1 1001 : Select AIN9 0010 : Select AIN2 1010 : Select AIN10 (PDP) 0011 : Select AIN3 1011 : Select AIN11 (PDM) 0100 : Select AIN4 10** : Stop use 0101 : Select AIN5 0110 : Select AIN6 0111 : Select AIN7	

Note: Please ensure that "1" is always written in the 7 bit of the A/D conversion control register. (ADCR)

A/D conversion value register

ADREG (FFDDH)

7	6	5	4	3	2	1	0
ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

(Initial value **** ****) read only

3.20 AMPLIFIER FOR SERVO CONTROL

The TMP90CR74A has the amplifier for CTL signal while playing, for CTL signal while recording (CTL amp) and for capstan FG signal (CFG amp). The amplified digital signal is input for capture CAP0, CAP2 through capture input circuit (CAPIN).

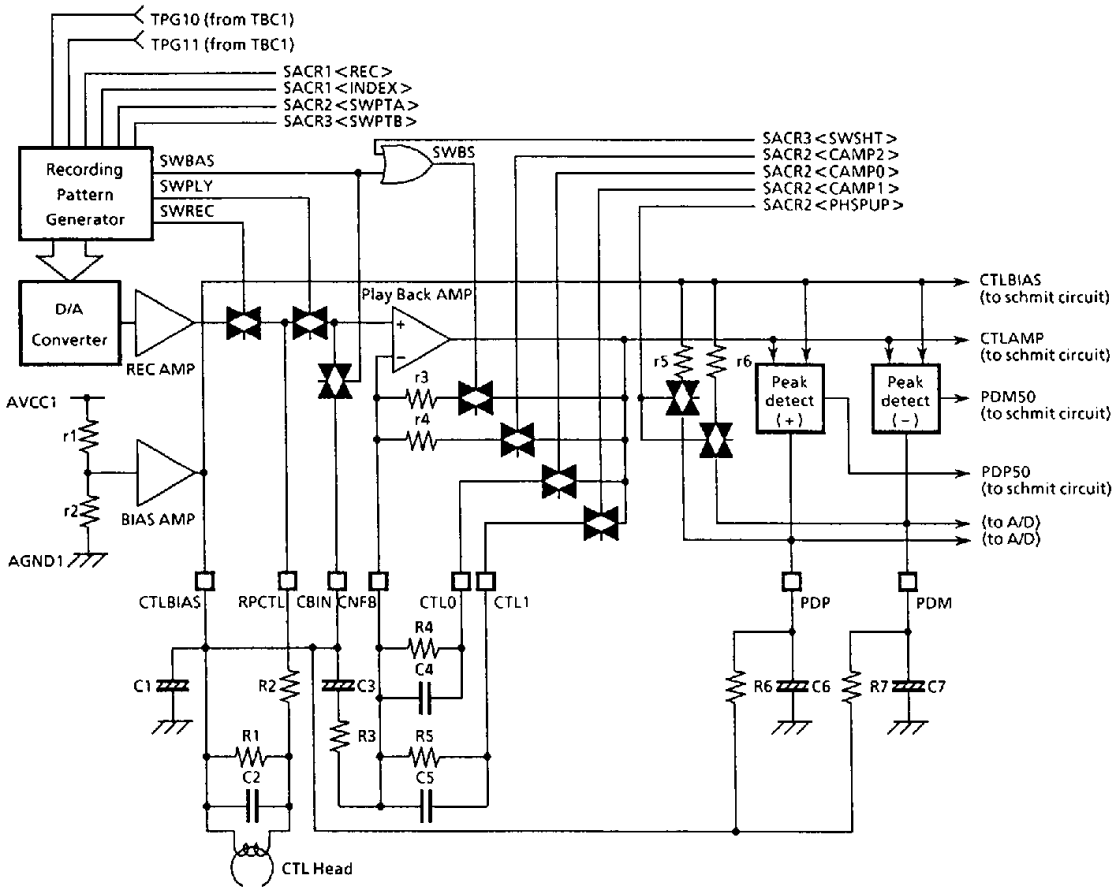
3.20.1 CTL Amp

(1) Configuration

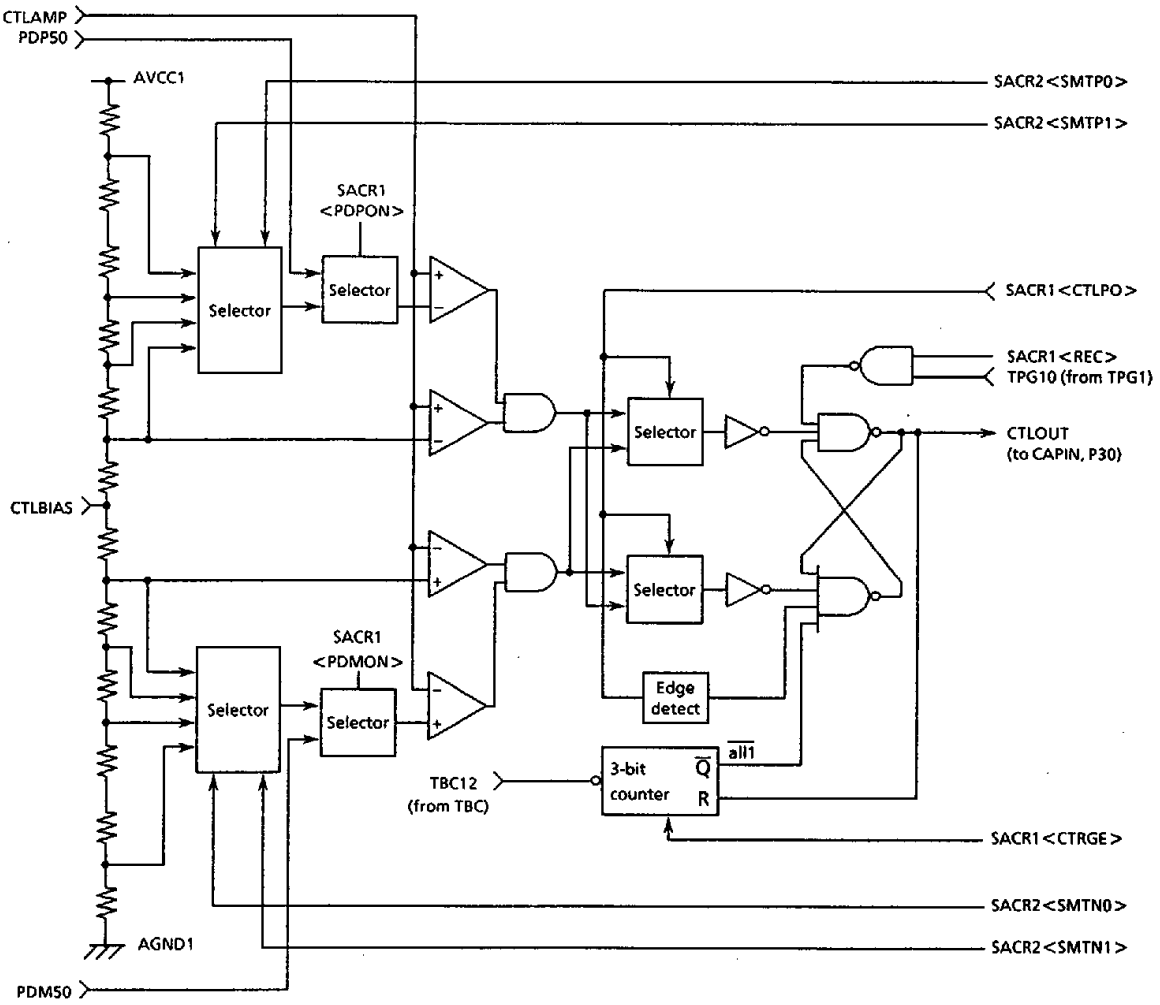
The CTL amplifier consists of right opeamplifier of CTL signal reproducing and schmit circuit, and D/A converter of CTL signal recording output.

Recording and reproducing of CTL signal and VISS/VASS signal can re-write by use to the CTL amplifier.

Figure 3.20.1 shown in configuration of CTL amplifier.



(a) Amplifier of playing, recording for CTL signal



(b) Schmit Circult

Fig 3.20.1 Configuration of Amplifier for Servo Control Circuit

(2) Control Registers

Servo amplifier control register 1

SACR1 (FFF1H)

7	6	5	4	3	2	1	0
IDIRE	DIRFLG	CTLPO	CTRGE	PDMON	PDPON	INDEX	REC

(Reset Value 0000 0000)

CTLPO	CTL polarity switch	0 : Forward 1 : Reverse	R/W
CTRGE	CTLOUT auto-reset enable/disable	0 : Disable 1 : Enable	
PDMON	CTL negative (−) schmit selection	0 : Manual 1 : Peak hold	
PDPON	CTL negative (+) schmit selection	0 : Manual 1 : Peak hold	
INDEX REC	CTL operation mode selection	00 : Reproducing mode *1 : Recording mode 10 : Index mode	

Servo amplifier control register 2

SACR2 (FFF2H)

7	6	5	4	3	2	1	0
PHSPUP	CAMP2	CAMP1	CAMP0	SMTP1	SMTP0	SMTN1	SMTN0

(Reset Value 0000 0000)

PHSPUP	Peak-hold recovery speed selection	0 : Normal recovery 1 : High speed recovery	R/W
CAMP2 to CAMP0	CTL reproduction amplifier switch	0 : OFF 1 : ON	
SMTP1 SMTP0	CTL negative (−) manual schmit level selection	00 : −100 [mV] 01 : −200 [mV] 10 : −300 [mV] 11 : −500 [mV]	
SMTN1 SMTN0	CTL negative (+) manual schmit level selection	00 : +100 [mV] 01 : +200 [mV] 10 : +300 [mV] 11 : +500 [mV]	

Servo amplifier control register 3

SACR3 (FFF3H)

7	6	5	4	3	2	1	0
IDIRS	SWPTB	SWPTA	AOUTS1	AOUTS0	CFGBS	CFGAS	SWSHT

(Reset Value 0000 0000)

SWPTB SWPTA	SWPB timing switch in index mode selection	00 : 1.5 [ms] 01 : 2.0 [ms] 10 : 2.5 [ms] 11 : 3.0 [ms]	R/W
AOUTS1 AOUTS0	CTLCFG (P30) output source selection	00 : CTL output 01 : CFGA output 10 : CFGB output 11 : −	
SWSHT	SWBS control	0 : Automatic control 1 : Forced "ON"	

Servo amplifier control register 4

SACR4 (F796H)	7	6	5	4	3	2	1	0	(Reset Value 0000 000*)
	"0"	"0"	"0"	"0"	CFGBZ	CFGAZ	CFGPO	CTLOUT	

CTLOUT	CTL reproduction amplifier output status	0 : CTL output = "0" 1 : CTL output = "1"	Read only

Note : Always write "0" in bit 4 to bit 7 of servo amplifier control register 4 (SACR4)

(3) Using the playback amp

(1) Gain switching

The reproduction CTL signal deriving from the magnetic head has its amplitude voltage in compliance with the tape speed. Consequently, if the amplifier gain is fixed, there is a possibility of its output becoming saturated. Furthermore, the output may be distorted by cut-off frequency settings. All these result in imperfect waveform reshaping, making it difficult to obtain exact duty cycle determination.

To prevent this problem, the reproducing amplifier allows you to set various constants using its internal feedback resistor or a feedback resistor connected external to the chip.

The gain and cut-off frequency can be set by using the <CAMP2 to CAMP0> in servo amplifier control register 2 (SACR2) and the <SWSHT> in servo amplifier control register 3 (SACR3).

During normal reproducing, you may set maximum gain and minimum cut-off frequency. During high-speed CUE/REV or FF/REW, however, you need to reduce the gain depending on the amplitude of the reproducing CTL signal. Furthermore, since the CTL signal frequency increases, set the cut-off frequency so as to comply with it.

As an example of constant settings, A fixed numbers that for normal reproducing, constants be set up using an external circuit via the CTL0/CTL1/CNFB pins. If the tape speed is very fast and the reproducing amplifier becomes saturated so you want to set a gain that is smaller than possible with an external circuit, you can use the internal feedback resistor. Refer to Section 4, "Electrical Characteristics" for details about the accuracy of this internal resistor.

(2) Schmit circuit

The reproducing amplifier output (CTLAMP signal) is waveform-reshaped using a Schmit circuit in two methods. In one, the Schmit level is set to 1/2 of the amplifier output level relative to the bias level; hence, this is called a peak-hold Schmit method. The other is called a manual Schmit method in which four fixed Schmit levels can be set. Each method allows you to set the Schmit level separately on the positive (+) and the negative (−) sides of the signal by using the <PDPON>, <PDMON> in servo amplifire control register 1 (SACR1). In either method, if the amplifier output is below the bias level ± 100 mV (when operating with AVCC1 = 5 V), Suhmit operation is canceled in order to prevent erratic device operation to noise.

The waveform-reshaped CTL signal (CTLOUT signal) is inputted to the capture input control circuit (CAPIN). In also can be output from the P30 (AMPOUT) pin. The CTLOUT signal can be monitored with the <CTLOUT> in servo amp control register 4 (SACR4).

a. Peak-hold Schmit method

Since the Schmit level is set to 1/2 of the peak level of reproducing amplifier output relative to the bias level, Schmit operation can be performed in compliance with level fluctuations of the reproducing CTL signal. If the tape speed is fast, the internal load resistors (r5 and r6) can be turned on using the <PHSPUP> in servo amplifier control register 2 (SACR2) to expedite the discharging time of the peak holders (PDP and PDM).

The voltage levels of the peak holders (PDP and PDM) can be monitored using the A/D converter.

b. Manual Schmit method

This method has four Schmit levels: ±100, ±200, ±300, and ±500 mV relative to the bias level (when operating with AVCC1 = 5 V) that can be set independently on each positive (+) and negative (−) side of the signal. Use the <SMTP1>, <SMTP0> in servo amp control register 2 (SACR2) to set the Schmit levels on the positive (+) side, use the SMTM1-0 bits to set the Schmit levels on the negative (−) side.

Use this manual Schmit method when the reproducing amplifier output level fluctuates greatly as in high-speed FF/REW and the peak-hold Schmit method cannot be used. Similarly, if the tape transport speed drops rapidly, the reproducing CTL signal deriving from the PB head has its amplitude reduced rapidly. Consequently, the amplitude of the reproducing amplifier output also is reduced, which depending on the time constants set on the peak-hold pins (PDP and PDM), makes recovery unable to comply with amplitude fluctuations. Therefore, when reducing the tape transport speed rapidly, switch to the manual Schmit method by estimating the reproducing amplifier output, because this method provides stable Schmit operation. Then, when the reproducing amplifier output level is peak-held, switch back to the peak-hold Schmit method.

Furthermore, if the transport speed of the tape on which the VISS/VASS signals are recorded increases and the playback CTL signal has a distorted waveform, set the Schmit width according to the DC fluctuations caused by the duty cycle of the signal.

(3) Switching Schmit polarity

When the direction of tape transport is reversed, the polarity of the reproducing CTL signal deriving from the PB head is inverted. This polarity switching ensures that the reference edges fed to the capture input control circuit (CPAIN), capture 0 (CAP0), VISS/VASS determination circuit (VIVA), and timer counter 2 (TC2) are always matched to the rising edge of the Schmit output.

Polarity switching is controlled by the <CTLPO> in servo amplifier control register 1 (SACR1). When the polarity is switched over, the Schmit output is reset low, waiting for input of the next reference edge.

(4) Retrigger function

During step slow reproducing, etc., it can happen that the Schmit output (CTLOUT signal) does not produce a negative (−) edge because the output level of tape's reproducing CTL signal drops. In such a case, you can set the <CTRGE> in servo amplifier control register 1 (SACR1), so that the Schmit output is reset low about $(2^{13}/fc) \times 7$ [s] after outputting a positive (+) edge without having to enter a negative (−) edge.

This retrigger function is also used when the CTL signal (CTLOUT) is fed to the capture 0 (CAP0) or timer counter 2 (TC2) during recording.

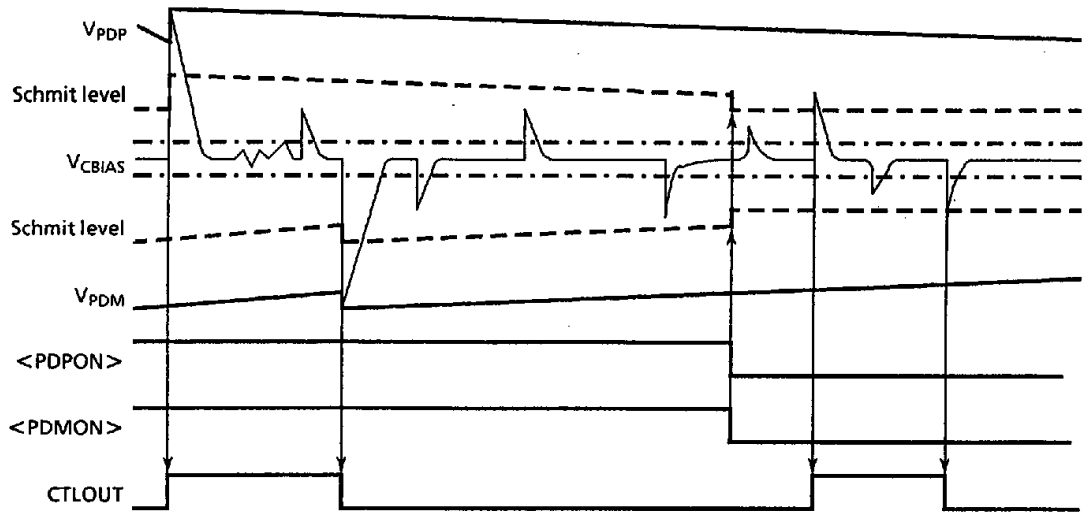


Fig 3.20.2 Timing Chart for PLY (playing) mode

(4) Using the record amplifier

The CTL signal recording amplifier can be used to output the recorded CTL signal or the VISS/VASS signal rewrite waveform during normal recording.

(1) Normal recording

By setting the <REC> in servo amplifier control register 1 (SACR1) to 1, it is possible to output a waveform of the same polarity as that of TPG10, output of the timing pulse generator 1 (TPG1). The recorded waveform output is started and ended synchronously with the TPG10 edges according to the set value of the REC bit as shown by the timing chart in Figure 3.20.3. The duty cycle can be set easily by patterning TPG10.

When normal recording is started, SWBAS turns on and SWPLY turns off and then SWREC turns on, causing the record amplifier to generate its output.

When recording is ended, each switch turns on or off with the reverse timing. This switchover timing is automatically controlled by the record pattern generating circuit. This switchover sequence prevents the reproducing amplifier output from going wild.

During normal recording, make sure that the reproducing amplifier gain is set to minimum.

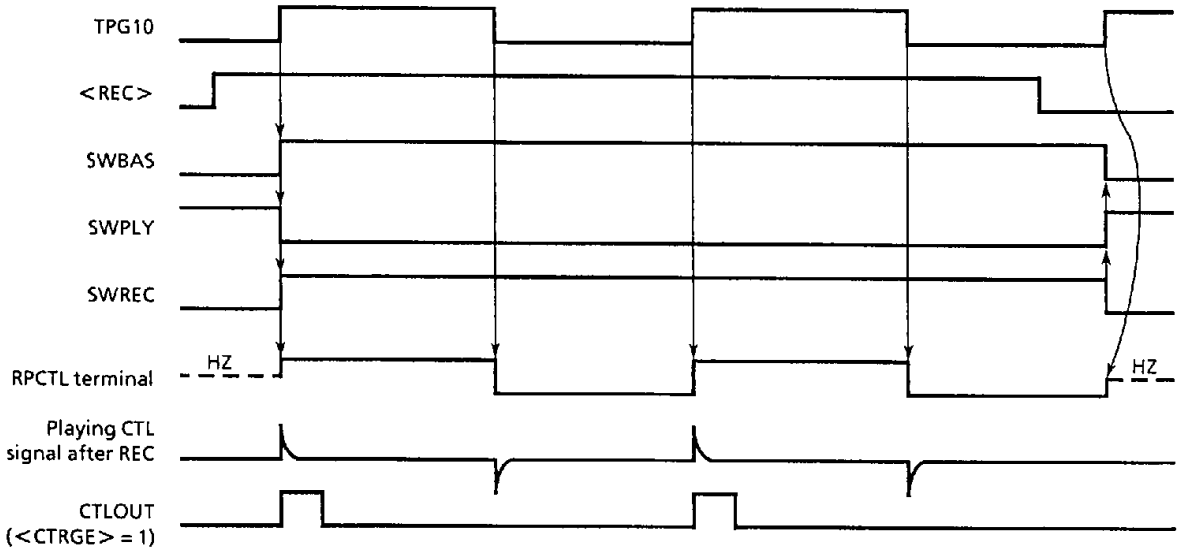


Fig 3.20.3 Timing Chart for REC (recording) mode

(2) Rewriting

When rewriting the CTL signal recorded on tape, operation is performed to rewrite only the negative (–) edges of the CTL signal (rewrite operation).

The rewrite operation is controlled using the timing pulse generator 1 (TPG1) outputs, TPG10 and TPG11, after setting the <INDEX> in servo amplifier control register 1 (SACR1) to 1 and REC bit to 0, as shown by the timing chart in Figure 3.20.4. The CTL signal negative (–) edge is written to by a falling edge of TPG10. Then, synchronously with the rising/falling edges of TPG11, the ramp level (CTL signal's positive (+) edge write mask) is output, performing an interval operation until the next negative (–) edge is written. Make sure that TPG10 and TPG11 are patterned so their rising edges occur at the same time.

Before a rewrite operation can be initiated, the INDEX bit must be set to 1 before TPG10 and TPG11 are pulsed high. Similarly, when a rewrite operation is completed, make sure that the PRCTL pin is placed in the high-impedance state by a falling edge of TPG11 before the INDEX is cleared to 0.

Since a rewrite operation involves repeatedly alternating record and reproduction, inductance in the control head can cause a voltage waveform to occur in the REC head after recording (rewrite) to back electromotive force which will be amplified by the reproducing amplifier. To prevent this problem, the reproducing amplifier can be disabled against input until the voltage waveform tails off. Use the <SWPTA>, <SWPTB> in servo amplifier control register 3 (SACR3) to set the duration of this disable time.

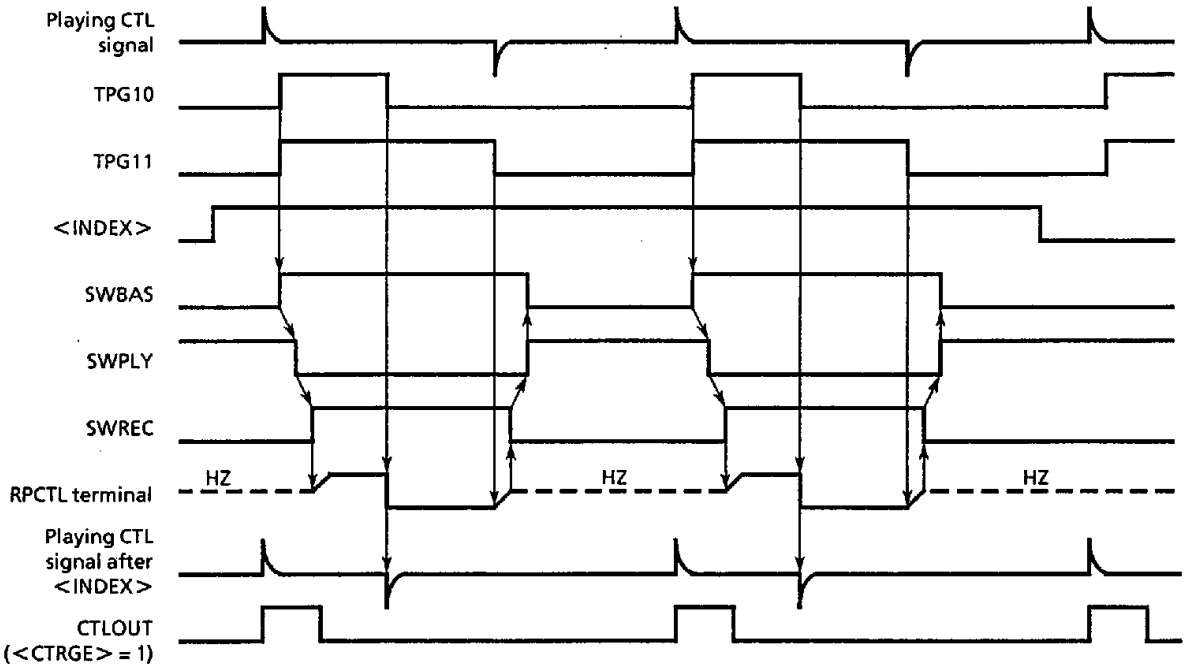
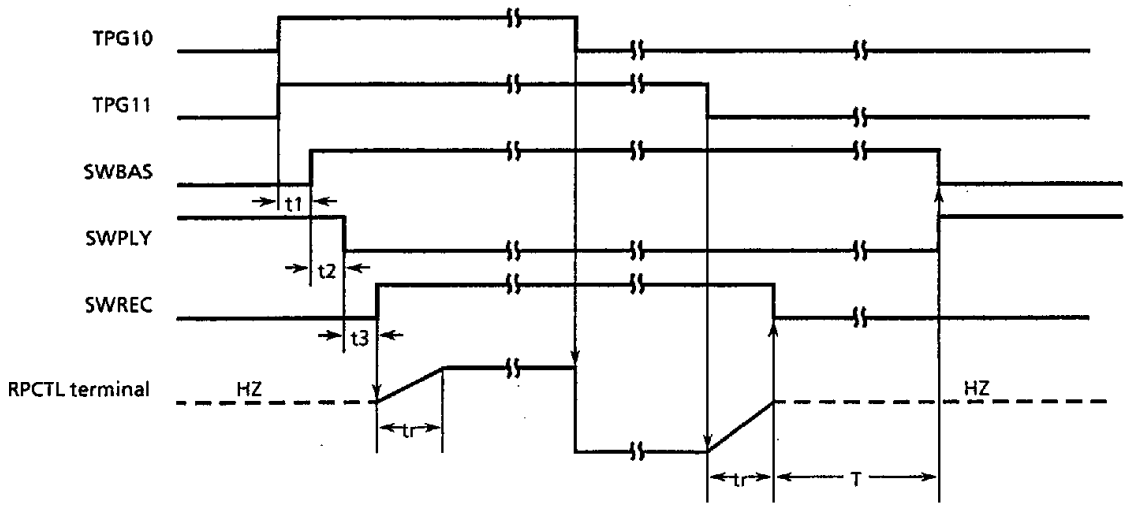


Fig 3.20.4 Timing chart for INDEX (Rewrite) ①



t1 = 0 to 64 μs
t2 = 64 μs
t3 = 64 μs
tr = 0.96 ms
T : Programmable (to be set on <SWPTB>, <SWPTA>)

Fig 3.20.5 Timing chart for INDEX (Rewrite) ②

3.20.2 CFG Amp

(1) Configration

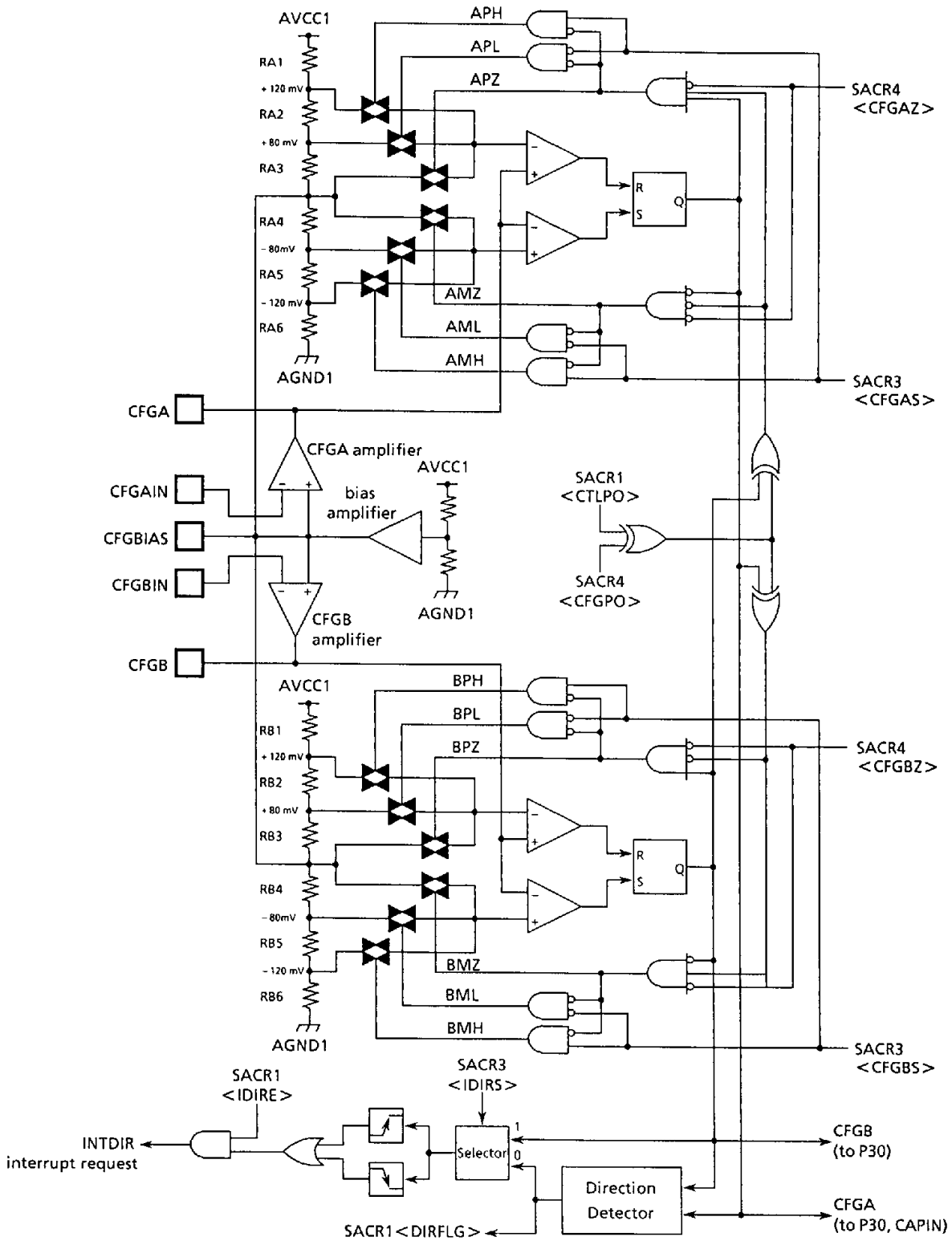


Fig 3.20.6 Configuration of CFG Amplifier

(2) Control Registers

Servo amplifier control register 1

SACR1 (FFF1H)

7	6	5	4	3	2	1	0
IDIRE	DIRFLG	CTLPO	CTRGE	PDMON	PDPON	INDEX	REC

(Reset Value 0000 0000)

IDIRE	INTDIR detect interrupt enable / disable	0 : Disable 1 : Enable	R/W
DIRFLG	DIR detect flag	0 : CFGB ahead of CFGA 1 : CFGA ahead of CFGB	Read only
CTLPO	CTL porarity switch	0 : Forward 1 : Reverse	R/W

Servo amplifier control register 3

SACR3 (FFF3H)

7	6	5	4	3	2	1	0
IDIRS	SWPTB	SWPTA	AOUT1	AOUT0	CFGBS	CFGAS	SWSHT

(Reset Value 0000 0000)

IDIRS	INTDIR interrupt source select	0 : DIRFLG 1 : CFGB	R/W
AOUT1 AOUT0	AMPOUT (P30) output source select	00 : CTL output (from CTL amplifier) 01 : CFGA output (from CFG amplifier) 10 : CFGB output (from CFG amplifier) 11 : –	
CFGBS	CFGB amplifier Schmit level select	0 : ±80 [mV] (at AVCC1 = 5 [V]) 1 : ±120 [mV] (at AVCC1 = 5 [V])	
CFGAS	CFGA amplifier Schmit level select		

Servo amplifier control register 4

SACR4 (F796H)

7	6	5	4	3	2	1	0
"0"	"0"	"0"	"0"	CFGBZ	CFGAZ	CFGPO	CTLOUT

(Reset Value 0000 000*)

CFGBZ	CFGB Schmit select	0 : Zero cross Schmit 1 : Manual Schmit	R/W
CFGAZ	CFGA Schmit select	0 : Zero cross Schmit 1 : Manual Schmit	
CFGPO	Zero cross polarity select	0 : Forward 1 : Reverse	

Note : Always write "0" in bit 7 to 4 of servo amplifier control register 4 (SACR4).

(3) CFG Amp Usage

The signal from a capstan motor is amplified by two inverting amplifier and is reformed by each Schmit trigger circuit. CFGA amplifier and CFGB amplifier are to be set gain / cutoff frequencies as normal operational amplifier.

① Schmit Circuit

There are two methods for CFGA / CFGB amplifier output Schmit. One is to set fixed level, called manual Schmit; the other is to reverse with bias-level, called zero-cross Schmit. One method is selected on <CFGAZ>, <CFGBZ> in servo amplifier control register 4 (SACR4).

a. Manual Schmit Trigger Circuit

The Schmit width can be selected from two, +/−80 mvolt or +/−120 mvolt based CFGBIAS level by setting <CFGAZ> and <CFGBZ> bits in SACR4 register. Usually this Schmit width is changed in accordance with noise level, but +/-80mvolt can be used for better condition to reduce the error of duty in AM modulation. If noise level is too big to get proper operation, use +/−120mvolt width.

b. Zero Cross Schmit Trigger Circuit

When two phase signals with 90 degree difference can be received from the capstan motor, these signals are proceeded through zero cross Schmit trigger circuit based on CFG BIAS by setting <CFGAZ> and <CFGBZ> bits in SACR4 register. In this case, the outputs and polarities of CFGA and CFGB signals can be controlled by setting <CTLPO> and <CFGPO> bits. The timing chart is shown in Fig 3.20.1. The combination for zero-cross Schmit function, results from phase relation between CFGA and CFGB, is described on the table below. Set <CFGPO> to "0" or "1" to match capstan FG architecture.
Changing the tape condition between forward and reverse generates INTDIR interrupt. Therefore, by shifting the polarity for CTL amp on <CTLPO> inside INTDIR routine, the zero cross Schmit for CFG amplifier can be operated continuously.

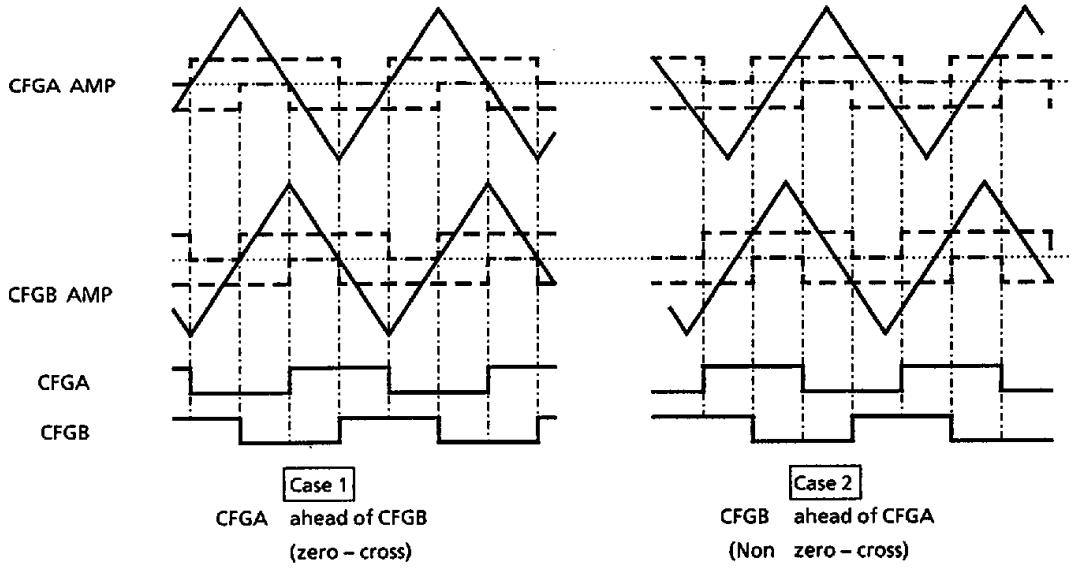
Table 3.20.1 FG phase and Schmit mode

<CFGPO>	<CTLPO>	CFGA amplifier input 90 deg ahead of CFGB	CFGB amplifier input 90 deg ahead of CFGA
0	0 (foward)	zero-cross Schmit	manual Schmit
	1 (reverse)	manual Schmit	zero-cross Schmit
1	0 (foward)	manual Schmit	zero-cross Schmit
	1 (reverse)	zero-cross Schmit	manual Schmit

Zero-cross Schmit can be operated if either side of CFGA amplifier or CFGB amplifier is set ; therefore they can operate by setting <CFGAZ> and <CFGBZ> respectively.
Figure 3.20.7 shown in sequence of zero-cross Schmit operation.

② Reverse Direction Detector

In the case that two phase signal with 90 degree difference changes its condition at changing between forward and reverse, the forward / reverse can be detected from CFGA and CFGB reformed signals by internal detector circuit. The result can be monitored by reading <DIRFLG> bit and the interrupt request INTDIR is generated when detected. Figure 3.20.8 shown is timingchart operation. Though <DIRFLG> is reset to "0" after reset, it is set to "1" if CFGA input has a phase ahead of CFGB input. The rising / falling edge of <DIRFLG> generates INTDIR interrupt. <IDIRE> is set INTDIR whether to enable or to disable. The source of INTDIR interrupt can be selected on <IDIRS> whether CFGB or DIRFLG.



Conditions : <CFGAZ> = <CFGBZ> = 0, <CFGPO> = <CTLPO>

Fig 3.20.7 CFG Amplifier Zero-cross Schmit Sequence

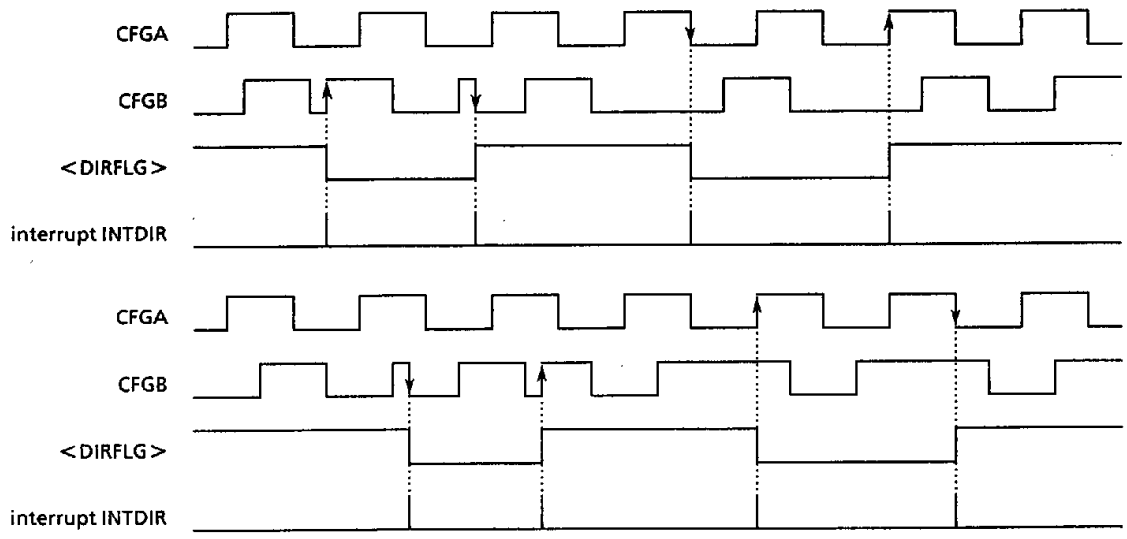


Fig 3.20.8 Forward / Reverse Detection Timing chart

3.21 PORT

The TMP90CS74 has 63 general-purpose digital I/O ports and 8 digital dedicated-function ports. Table 3.21.1 indicates the digital port structure.

Table 3.21.1 General-purpose I/O Ports and Dedicated-function Ports

Type	Port Name	Bit Structure	Number of Pins
General-purpose I/O Ports	Port 0	P07 to P00	8
	Port 1	P17 to P10	8
	Port 2	P27 to P20	8
	Port 3	P37 to P30	8
	Port 4	P47 to P40	8
	Port 5	P57 to P50	8
	Port 6	P67 to P60	8
	Port 7	P74 to P70	5
	Port 8	P81 to P80	2
Dedicated-function Ports	Pulse-width modulation	PWM1, PWM0	2
	Head switch signal output	VASWP	1
	OSD oscillator connection pins	XI, XO	2
	Vertical sync signal input	VDIN	1
	Composite sync signal input	CSYNC	1
	Clock output	CLK	1

(1) I/O Settings

Each bit of port 0 to port 8 can be set for input or output.

(2) Output Circuit Format Settings

Pins P20 to P24, P37, P52 and P53, P55 and P56, P74, PWM0 and PWM1 can be programmed as push-pull outputs or N-channel open drain outputs by software.

(3) Output Control in STOP mode

Except for the XI, XO, VDIN, and CSYNC pins all digital ports can set whether the output state in STOP mode remains or turns to high-impedance by setting <DRVE> in the watch dog timer control register 1 (WDTCR1) (see Section 3.2, "System Clock Control Circuit").

Figure 3.21.1 shows the port output control circuit in STOP mode.

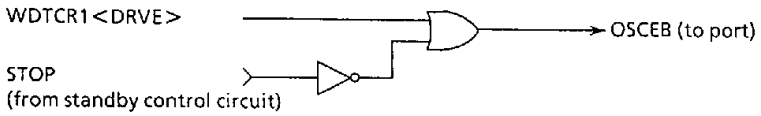


Fig 3.21.1 Port Output Control Circuit in STOP Mode

3.21.1 Port 0 (P00 to P07)

Port 0 is an 8-bit general-purpose I/O port which can specify input/output in bit unit. The control register (P0CR) is used to set input/output.

Reset operations clear P0 port data register (P0) and P0 port control register (P0CR) to "0" and initialized to the input mode.

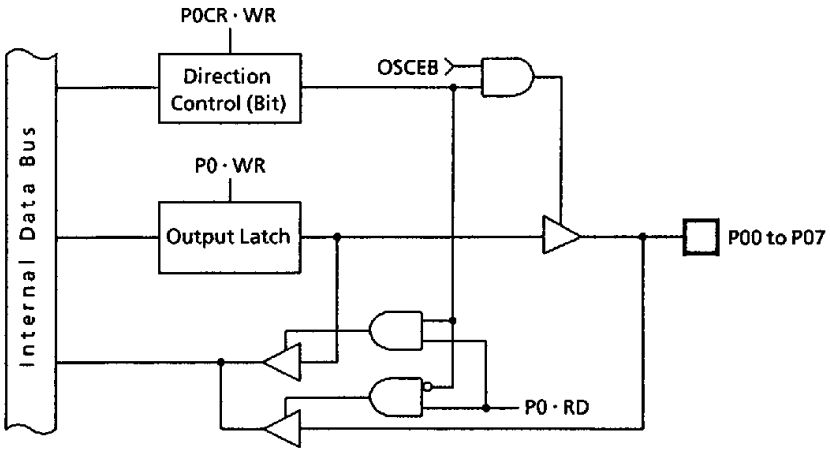


Fig 3.21.2 Port 0 (P07 to P00) Block Diagram

Port 0 Data Register

P0 (FFC0H)

7	6	5	4	3	2	1	0
P07	P06	P05	P04	P03	P02	P01	P00

(Reset Value 0000 0000) (R/W)

Port 0 Control Register 1

P0CR (FFC1H)

7	6	5	4	3	2	1	0
P07C	P06C	P05C	P04C	P03C	P02C	P01C	P00C

(Reset Value 0000 0000)

P07C to P00C	Port 0 Input / Output control (per bit)	0 : Input 1 : Output	write only

3.21.2 Port 1 (P17 to P10)

Port 1 is an 8-bit general-purpose I/O port which can specify input/output in bit unit. The control register (P1CR) is used to set input/output.

Reset operations clear P1 port data register (P1) and P1 port control register (P1CR) to "0" and initialized to the input mode.

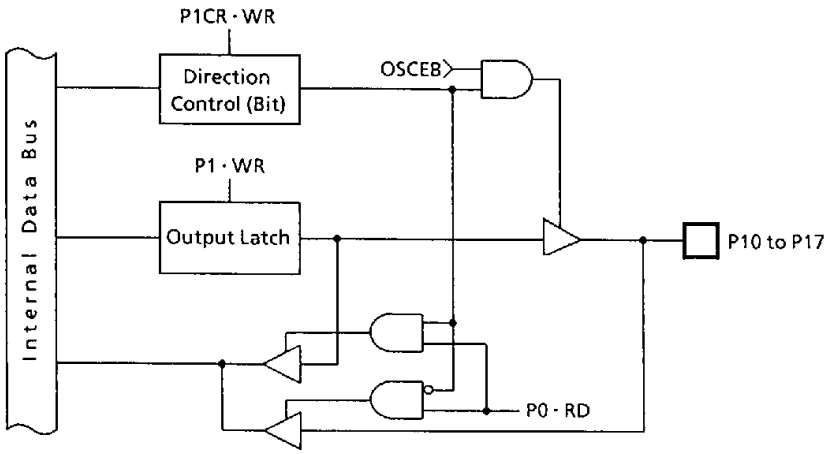


Fig 3.21.3 Port 1 (P17 to P10) Block Diagram

Port 1 Data Register

P1 (FFC2H)	7	6	5	4	3	2	1	0
	P17	P16	P15	P14	P13	P12	P11	P10

(Reset Value 0000 0000) (R/W)

Port 1 Control Register 1

P1CR (FFC3H)	7	6	5	4	3	2	1	0
	P17C	P16C	P15C	P14C	P13C	P12C	P11C	P10C

(Reset Value 0000 0000)

P17C to P10C	Port 1 Input / Output control (per bit)	0 : Input 1 : Output	write only

3.21.3 Port 2 (P27 to P20)

Port 2 is an 8-bit general-purpose I/O port which can specify input/output in bit unit. The control register (P2CR) is used to set input/output.

Reset operations clear P2 port data register (P2) and P2 port control register (P2CR) to "0" and initialized to the input mode.

(1) P20 (TPG00/TP0)

P20 used as an TPG00 of timng pulse generator 0 (TPG0) output, and also timing pulse output (TP0). When P20 is used as TPG00 or TP0, setting <P20C> in port 2 controlregister (P2CR) to "1" to select output mode.

The output circuit of P20 can be selected either push-pull output or N-channel open drain output by setting <P20OC> in open drain control register1 (ODMCR1).

① TPG00

TPG00 is output by clearing <P20> of the port 2 data register (P2) to "0", then setting <TPG00E> of the port 2 mode register (P2MR) to "1".

② TP0

The data written to <TP0D> in the TP data register (TPDR) can be output in sync with the rising or falling edge of TPG01 or TPG03 in the TPG0 output.

When P20 is used as used as an to TP0, setting <TP0E> of P2MR to "1" and set the output trigger to TPG01 or TPG03 by setting <VASEL0> of the TP control register (TPCR), then select the edge using <TPE0>.

(2) P21 (TPG01/TP1)

P21 used as an TPG01 of timng pulse generator 0 (TPG0) output, and also timing pulse output (TP1). When P21 is used as TPG01 or TP1, setting <P21C> in port 2 controlregister (P2CR) to "1" to select output mode.

The output circuit of P21 can be selected either push-pull output or N-channel open drain output by setting <P21OC> in open drain control register1 (ODMCR1).

① TPG01

TPG01 is output by clearing <P21> of the port 2 data register (port 2) to "0", then setting <TPG01E> of the port 2 port mode register (P2MR) to "1".

② TP1

The data written to <TP1D> in the TP data register (TPDR) can be output in sync with the rising or falling edge of TPG01 or TPG03 in the TPG0 output.

When P21 used as TP1, setting <TP1E> of P2MR to "1" and set the output trigger to TPG01 or TPG03 by setting <VASEL1> of the TP control register (TPCR), then select the edge using <TPE1>.

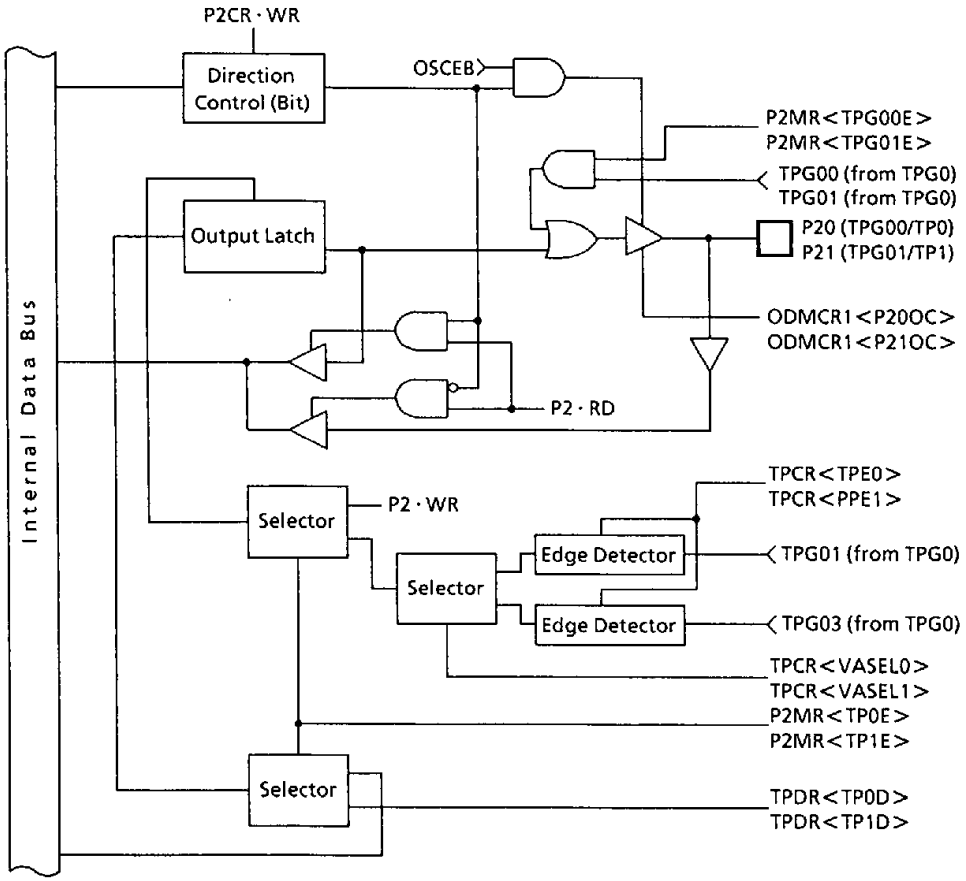


Fig 3.21.4 Port 2 (P20 and P21) Block Diagram

(3) P22 (CR/VTP3)

P22 used as color rotary output (CR), and also timng pulse (VTP3). When P22 is used as CR or VTP3, setting <P22C> in port 2 control register (P2CR) to "1" to select output mode.

The output circuit of P22 can be selected either push-pull outputor N-channel open drain output by setting <P22OC> in open drain control register1 (ODMCR1).

① CR

The CR is output by clearing <P22> of the port 2 data register(P2) to "0", then setting <CRMOD> of head amp control register (HACR) to "1".

② VTP3

The data written to <VTP3D> of the TP data register (TPDR) can be output in sync with the rising or falling edge of TPG03 in the timing pulse generator 0 (TPG0) output.

When P22 is used as VTP3, setting <VTP3E> of the port 3 mode register (P3MR) to "1", then set <VTPE34> of HACR to select the rising or falling edge of TPG03.

(4) P23 (HA/VTP4)

P23 used as an head amp output (HA),and also timing pulse output (VTP4). When P23 is used as HA or VTP4, setting <P23C> in port 2 control register (P2CR) to "1" to select output mode.

The output circuit of P23 can be selected either push-pull outputor N-channel open drain output by setting <P23OC> in open drain control register1 (ODMCR1).

① HA

The HA is output by clearing <P23> of the port 2 data register (P2) to "0", then setting <CRMOD> of head amp control register (HACR) to "1".

② VTP4

The data written to <VTP4D> of the port P7 data register (port 7) can be output in sync with the rising or falling edge of TPG03 in the timing pulse generator 0 (TPG0) output.

When P23 is used as VTP4, setting <VTP4E> of the port 3 mode register (P3MR) to "1", then set <VTPE34> of HACR to select the rising or falling edge of TPG03.

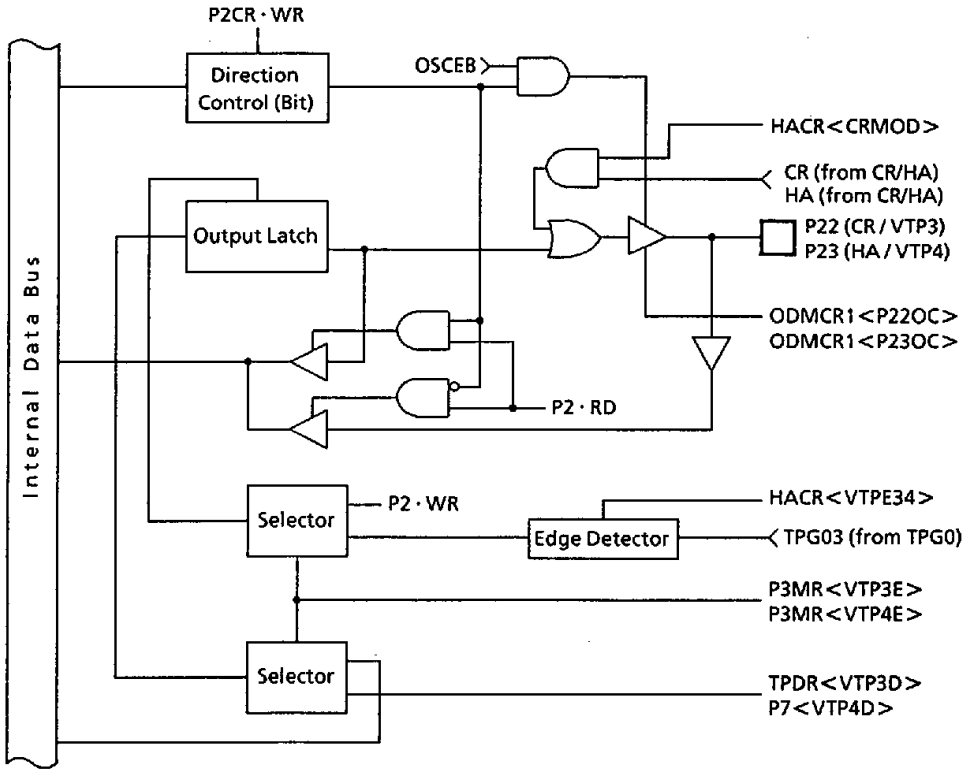


Fig 3.21.5 Port2 (P22 and P23) Block Diagram

(5) P24 (TP2/TI3)

P24 used as an timng pulse output (TP2) and also event counter input (TI3).

When P24 is used as TI3 or TP2, setting <P24C> in port 2 control register (P2CR) to "1" to select output mode.

The output circuit of P24 can be selected either push-pull output orN-channel open drain output by setting <P20OC> in open drain control register1 (ODMCR1).

① TP2

The data written to <TP2D> of the TP data register (TPDR) can be output in sync with the rising or falling edge of TPG01 or TPG03 in TPG0 output.

When P24 is used as TP2, setting <TP2E> of the port 2 mode register (P2MR) to "1", then set <VASEL2> of the TP control register (TPCR) to select TPG01 or TPG03 as the output trigger, then set <TPE2> to select the edge.

② TI3

This is the event count input for timer counter 3 (TC3).

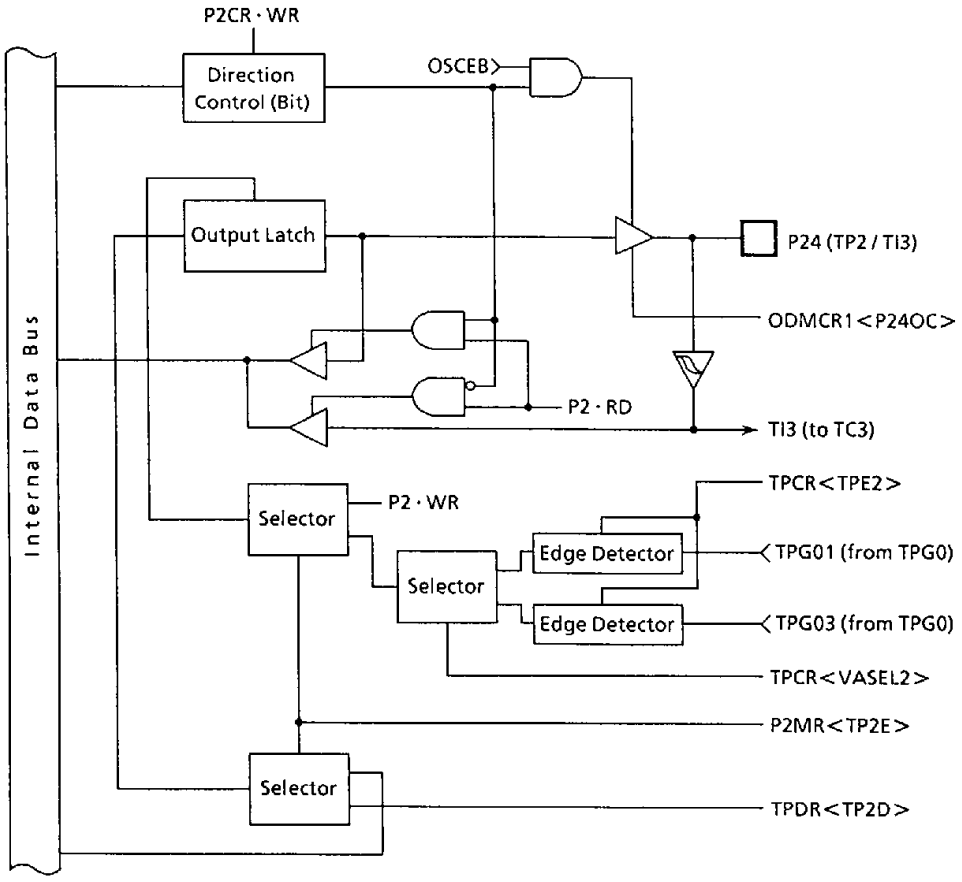


Fig 3.21.6 Port2 (P24) Block Diagram

(6) P25 (SCLK0)

P25 used as an serial clock input/output (SCLK0) of serial channel (SIO0).

When P25 is used as serial clock output, setting <P25C> in port 2 control register (P2CR) to "1" to select output mode. The output circuit of P25 can be selected either push-pull output or N-channel open drain output by setting <P25OC> in open drain control register1 (ODMCR1).

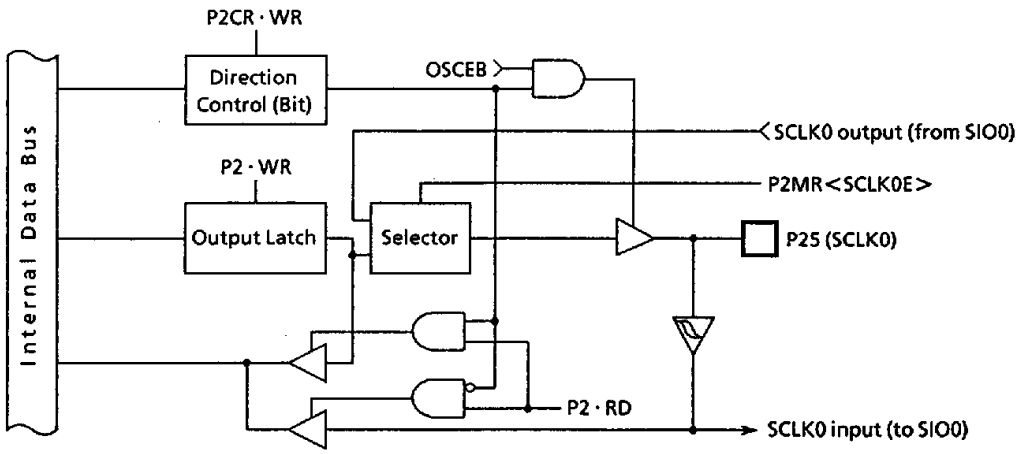


Fig 3.21.7 Port 2 (P25) Block Diagram

(7) P26 (TXD0)

P26 also used as an serial data output (TXD0) of serial chanel (SIO0).

When P26 is used as serial data output, setting <P26C> in port 2 control register (P2CR) to "1" to select output mode,and setting <TXD0E> of port 2 mode register (P2MR) to "1".

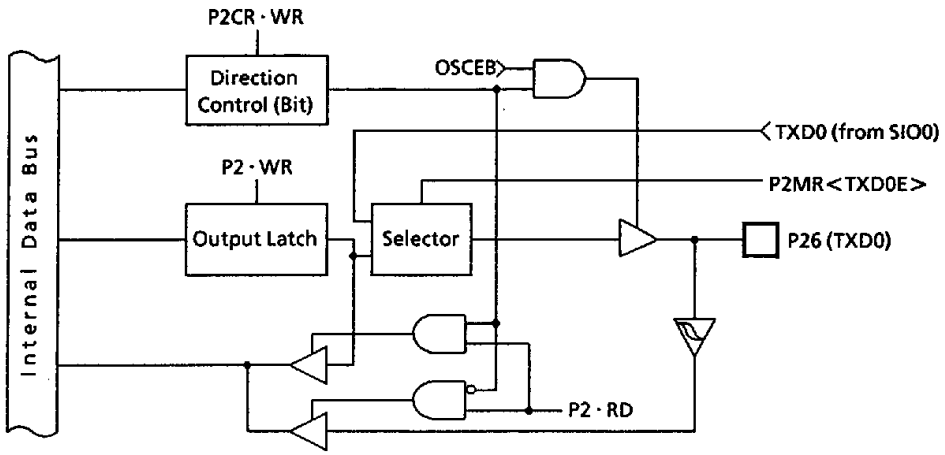


Fig 3.21.8 Port 2 (P26) Block Diagram

(8) P27 (RXD0)

P27 also used as an serial data output (RXD0) of serial chanel (SIO0).
When P27 is used as serial data input, clearing <P27C> in port 2 control register (P2CR) to "0" to select input mode, and set <RXD0E> of port 2 mode register (P2MR) to "1".

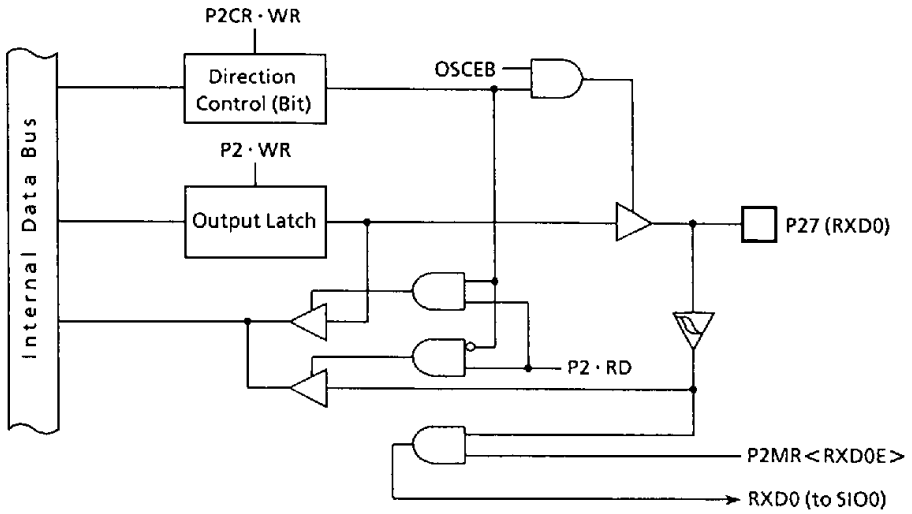


Fig 3.21.9 Port 2 (P27) Block Diagram

Port 2 Data Register

P2 (FFC4H)

7	6	5	4	3	2	1	0
P27	P26	P25	P24	P23	P22	P21	P20

(Reset Value 0000 0000) (R/W)

Port 2 Control Register

P2CR (F780H)

7	6	5	4	3	2	1	0
P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C

(Reset Value 0000 0000)

P27C to P20C	Port2 Input / Output control (per bit)	0 : Input 1 : Output	(R/W)

Port 2 Mode Register

P2MR (F781H)

7	6	5	4	3	2	1	0
RXD0E	TXD0E	SCLK0E	TP2E	TP1E	TP0E	TPG01E	TPG00E

(Reset Value 0000 0000)

RXD0E	RXD0 input enable/disable	0 : Disabled 1 : Enabled	(R/W)
TXD0E	TXD0 output enable/disable	0 : Disabled 1 : Enabled	
SCLK0E	SCLK0 I/O enable/disable	0 : Disabled 1 : Enabled	
TP2E	TP2 output enable/disable	0 : Disabled 1 : Enabled	
TP1E	TP1 output enable/disable	0 : Disabled 1 : Enabled	
TP0E	TP0 output enable/disable	0 : Disabled 1 : Enabled	
TPG01E	TPG01 output enable/disable	0 : Disabled 1 : Enabled	
TPG00E	TPG00 output enable/disable	0 : Disabled 1 : Enabled	

Port 3 Mode Register

P3MR (F783H)

7	6	5	4	3	2	1	0
VTP4E	VTP3E	CAPFRD	CAPFR	TPG12E	TP3E	T03E	CTLCFG

(Reset Value 0000 0000)

VTP4E	VTP4 output enable/disable	0 : Disable 1 : Enable	R/W
VTP3E	VTP3 output enable/disable	0 : Disable 1 : Enable	

TP Control Register

TPCR (FFDAH)

7	6	5	4	3	2	1	0
TP3E	VASEL3	TPE2	VASEL2	TPE1	VASEL1	TPE0	VASEL0

(Reset Value 0000 0000)

TPE2	TP2 (P24) Trigger Edge Selection	0 : Rising Edge 1 : Falling Edge	R/W
VASEL2	TP2 (P24) Trigger Selection	0 : TPG03 1 : TPG01	
TPE1	TP2 (P21) Trigger Edge Selection	0 : Rising Edge 1 : Falling Edge	
VASEL1	TP2 (P21) Trigger Selection	0 : TPG03 1 : TPG01	
TPE0	TP0 (P20) Trigger Edge Selection	0 : Rising Edge 1 : Falling Edge	
VASEL0	TP0 (P20) Trigger Selection	0 : TPG03 1 : TPG01	

TP Data Register

TPDR (FFDBH)

7	6	5	4	3	2	1	0
VTP3D	VTP2D	VTP1D	VTP0D	TP3D	TP2D	TP1D	TP0D

(Reset Value 0000 0000)

VTP3D	VTP3 (P22) Data Register		R/W
TP2D	TP2 (P24) Data Register		
TP1D	TP1 (P21) Data Register		
TP0D	TP0 (P20) Data Register		

P7 Data Register

P7 (FFDBH)

7	6	5	4	3	2	1	0
		VTP4D	P74	P73	P72	P71	P70

(Reset Value **00 0000)

VTP4D	VTP4 (P23) Data Register		R/W

Head Amp Control Register

HACR (F794H)

7	6	5	4	3	2	1	0
CRMOD	"0"	VTPE34	DFFP01	DFFP00	COMP SEL	CRP0	HAP0

(Reset Value 0000 0000)

CRMOD	CR (P22) output, HA (P23) output, COMPIN (P43) input enable/disable	0 : Disable 1 : Enable	R/W
VTPE34	VTP3 (P22) / VTP4 (P23) Trigger Edge Selection	0 : Rising Edge 1 : Falling Edge	

Note : Please ensure that "0" is always written in the 6 bit of the Head Amp Control Register (HACR).

Open Drain Mode Control Register 1

ODMCR1 (F789H)

7	6	5	4	3	2	1	0
PWM 1OC	PWM 0OC	P37OC	P24OC	P23OC	P22OC	P21OC	P20OC

(Reset Value 0000 0000)

P24OC	P24 Open Drain Control	0 : Push-pull Output 1 : Open Drain Output	R/W
P23OC	P23 Open Drain Control		
P22OC	P22 Open Drain Control		
P21OC	P21 Open Drain Control		
P20OC	P20 Open Drain Control		

3.21.4 Port 3 (P37 to P30)

Port 3 is an 8-bit general-purpose I/O port which can specify input/Output in bit unit. The control register (P3CR) is used to set input/output.

Reset operations clear P3 port data register (P3) and P3 port control register (P3CR) to "0" and initialized to the input mode.

(1) P30 (AMPOUT)

P30 also used as the servo amp output (AMPOUT).

AMPOUT can be used to output the CTL amp reproduction amplifier output (the CTLOUT signal), the CFG amplifier CFGA amplifier output (the CFGA signal), or the CFGB amplifier output (the CFGB signal) by setting <AOUTS1 and AOUTS0> of the servo amplifier control register (SACR3).

When P30 is used as an AMPOUT, set <P30C> of the port 3 control register (P3CR) to "1" to select output mode, then write "0" to <P30> of the port 3 data register (P3).

AMPOUT is output by setting <CTLCFGE> of the port 3 mode register (P3MR) to "1".

By setting <P30C> to input mode, P30 can be used to input an externally shaped CTL (CTLIN) signal. CTLIN is input to the capture input control circuit (CAPIN) and allows capture 0 (CAP0) to measure the frequency periodically.

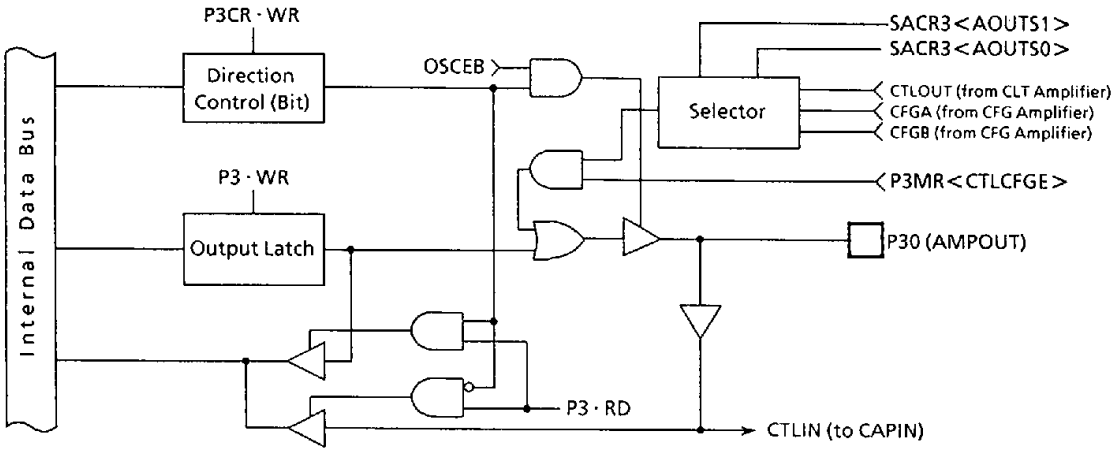


Fig 3.21.10 Port 3 (P30) Block Diagram

(2) P31 (DFGPG)

P31 also used as the head cylinder speed and phase signal (DFGPG) input.

When P31 is used as an DFGPG input, clearing <P31C> of the port 3 control register (P3CR) to "0" to select input mode.

(3) P32 (RMTIN)

P32 also used as the remote control signal (RMTIN) input.

When P32 is used as an RMTIN input, clearing <P32C> of the port 3 control register (P3CR) to "0" to select input mode.

(4) P33 (ACCK)

P33 also used as the AC clock (ACCK) input.

When P33 is used as an ACCK input, clearing <P33C> of the port 3 control register (P3CR) to "0" to select input mode.

(5) P34 (TC0/EXT)

P34 used as the event count input (TI0) for timer counter 0 (TCO), and also the external trigger input (EXT) for capture 0 (CAP0).

When P34 is used as TI0 input or EXT input, clearing <P34C> of the port 3 control register (P3CR) to "0" to select input mode.

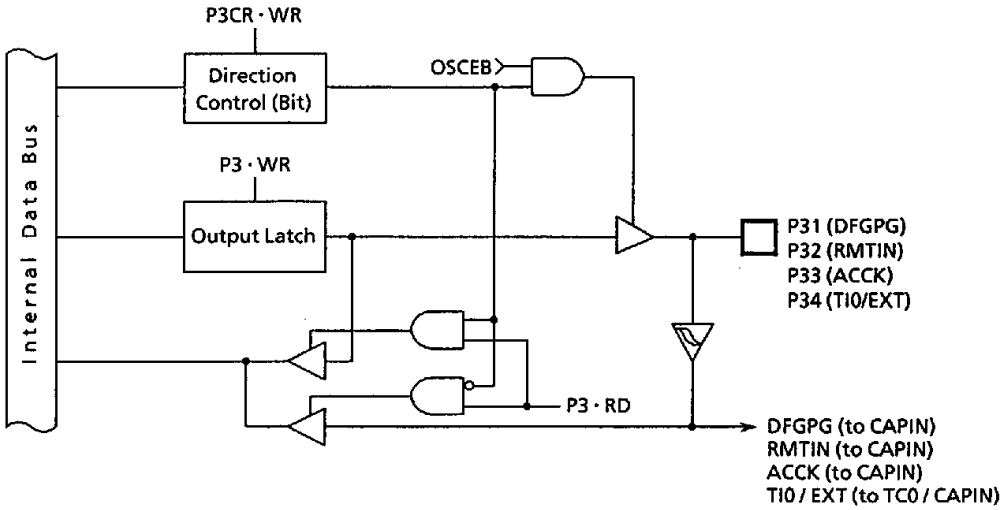


Fig 3.21.11 Port 3 (P31, P32, P33 and P34) Block Diagram

(6) P35 (TI2/TO3)

P35 used as the event count input (TI2) of timer counter 2 (TC2), and also the timer flip-flop output (T03) of timer counter 3 (TC3).

When P35 is used as TI2, clear <P35C> of the port 3 control register (P3CR) to "0" to select input mode.

When (P35 is used as TO3 output, write "0" to <P35> of the port P3 data register (P3), then set <P35C> of P3CR to "1" to select output mode. TO3 is output by setting <T03E> of the port 3 mode register (P3MR) to "1".

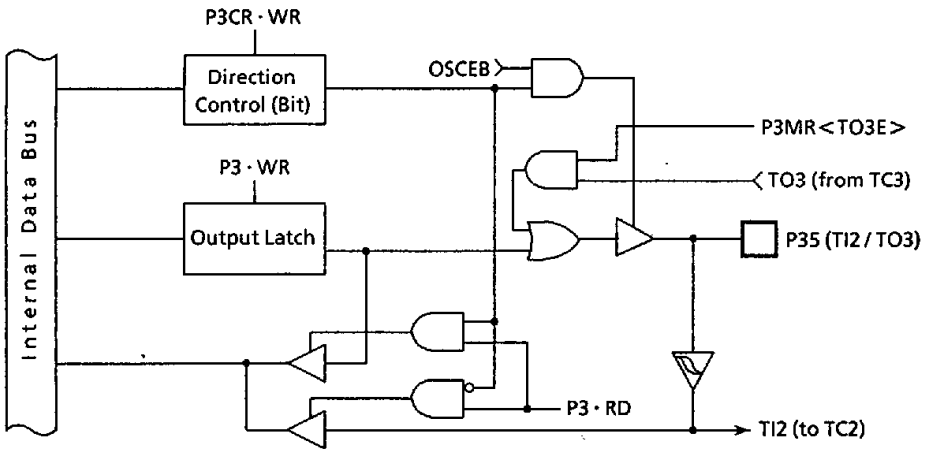


Fig 3.21.12 Port 3 (P35) Block Diagram

(7) P36 (TPG12/TP3)

P36 also used as the TPG12 of timing pulse generator 1 (TPG1) output, and also timing pulse output (TP3).

When used as TPG12 or TP3 set <P36C> of the port 3 control register (P3CR) to "1" to select output mode.

① TPG12

TPG12 is output by clearing <P36> of the port 3 data register (port 3) to "0", then setting <TPG12E> of the port 3 mode register (P3MR) to "1".

② TP3

The data written to <TP3D> of the TP data register (TPDR) can be output in sync with the rising or falling edge of TPG01 or TPG03 in the TPG0 output.

When P36 is used as TP3 output, setting <TP3E> of P3MR to "1", and set the output trigger to TPG01 or TPG03 by setting <VASEL3> of the TP control register (TPCR), then select the edge using <TPE3>.

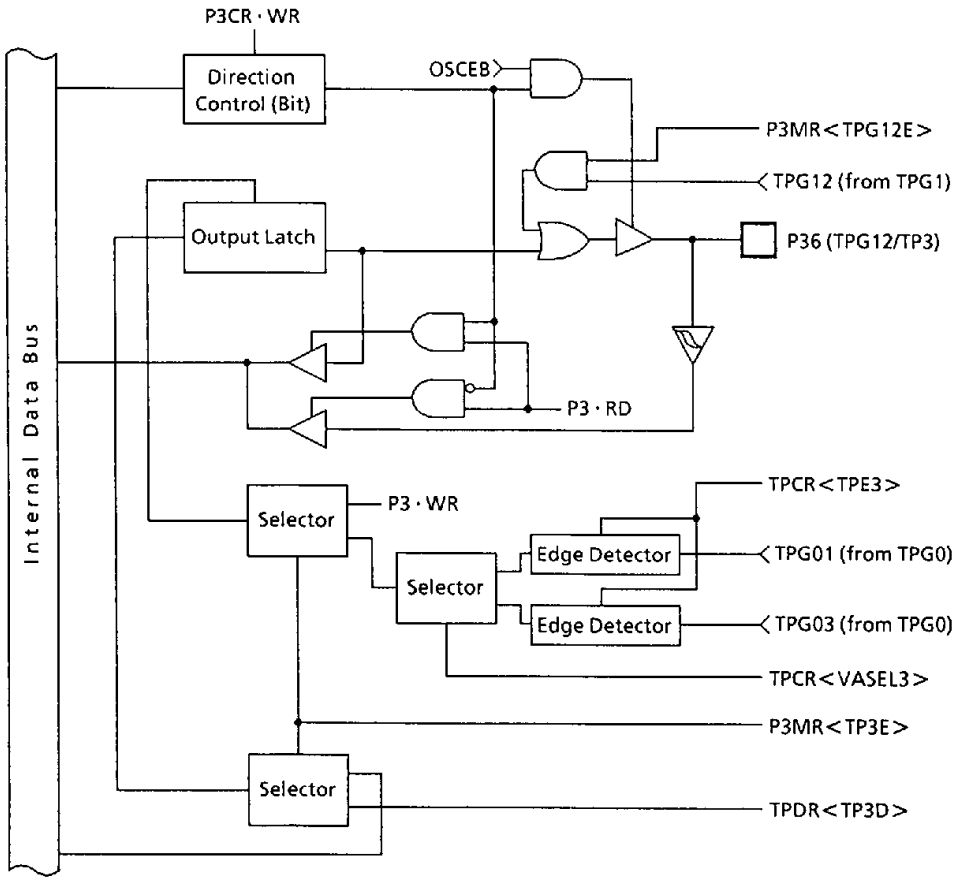


Fig 3.21.13 Port 3 (P36) Block Diagram

(8) P37 (CAPFR)

P37 also used as the capstan motor direction control pulse output (CAPFR).

The data in <CAPFRD> of the port 3 mode register (P3MR) can be output in sync with the rising or falling edge of the 12-bit pulse width modulation output 0 (PWM0). By assigning PWM0 output to the DC conversion output of the speed/phase error for the capstan servo system, the capstan motor direction can be controlled by the CAPFR output.

When P37 is used as CAPFR, set <P37C> of the port 3 control register (P3CR) to "1" to select output mode, then set <CAPFR> of P3MR to "1". The PWM0 edge select by setting <CFRTRGS> of the PWM control register (PWMCR).

The output circuit can be set to push-pull output or N-channel open drain output by setting <P37OC> in the open drain control register 1 (ODMCR1).

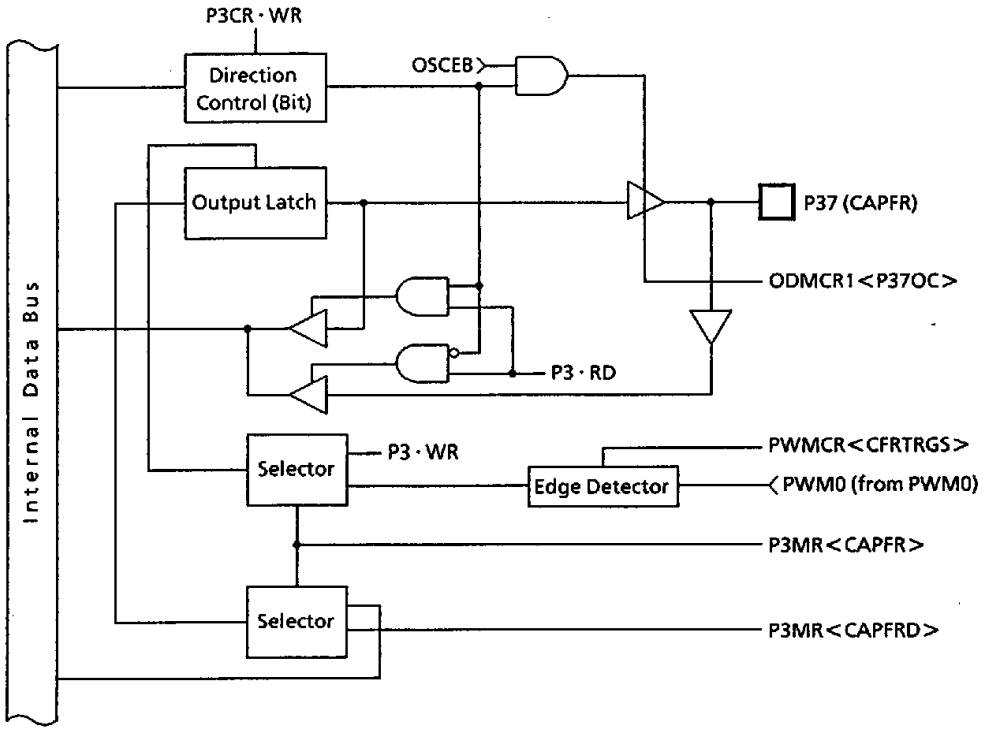


Fig 3.21.14 Port 3 (P37) Block Diagram

Port 3 Data Register

P3 (FFC5H)	7	6	5	4	3	2	1	0	(Reset Value 0000 0000) (R/W)
	P37	P36	P35	P34	P33	P32	P31	P30	

Port 3 Control Register

P3CR (F782H)	7	6	5	4	3	2	1	0	(Reset Value 0000 0000)
	P37C	P36C	P35C	P34C	P33C	P32C	P31C	P30C	

P37C to P30C	Port 3 Input/Output control (per bit)	0 : Input 1 : Output	(R/W)

Port 3 Mode Register

P3MR (F783H)

7	6	5	4	3	2	1	0
VTP4E	VTP3E	CAPFRD	CAPFR	TPG12E	TP3E	TO3E	CTLC FGE

(Reset Value 0000 0000)

CAPFRD	CAPFR (P37) Data Register		R/W
CAPFR	CAPFR (P37) output enable/disable	0 : Disabled 1 : Enabled	
TPG12E	TPG12 (P36) output enable/disable	0 : Disabled 1 : Enabled	
TP3E	TP3 (P36) output enable/disable	0 : Disabled 1 : Enabled	
TO3E	T03 (P35) output enable/disable	0 : Disabled 1 : Enabled	
CTLCFGE	AMPOUT (P30) output enable/disable	0 : Disabled 1 : Enabled	

Servo Amp Control Register 3

SACR3 (FFF3H)

7	6	5	4	3	2	1	0
IDIRS	SWPTB	SWPTA	AOUTS1	AOUTS0	CFGBS	CFGAS	SWSHT

(Reset Value 0000 0000)

AOUTS1 AOUTS0	AMPOUT (P30) Output Source Select	00 : CTLOUT Output (from CTL amplifier) 01 : CFGA Output (from CFG amplifier) 10 : CFGB Output (from CFG amplifier) 11 : Don't Use	R/W

PWM Control Register

PWMCR (F793H)

7	6	5	4	3	2	1	0
	PWM12 MOD	CFRT RGS	CSYN CPO	PWM SEL	PWM02	PWM01	PWM00

(Reset Value *000 0000)

CFRTRGS	CAPFR (P37) Trigger Edge Selection	0 : Rising Edge 1 : Falling Edge	R/W

TP Control Register

TPCR (FFDAH)

7	6	5	4	3	2	1	0
TPE3	VASEL3	TPE2	VASEL2	TPE1	VASEL1	TPE0	VASEL0

(Reset Value 0000 0000)

TPE3	TP3 (P36) Trigger Edge Selection	0 : Rising Edge 1 : Falling Edge	R/W
VASEL3	TP3 (P36) Trigger Selection	0 : TPG03 1 : TPG01	

TP Data Register

TPDR (FFDBH)

7	6	5	4	3	2	1	0
VTP3D	VTP2D	VTP1D	VTP0D	TP3D	TP2D	TP1D	TP0D

(Reset Value 0000 0000)

TP3D	TP3 (P36) Data Register		R/W

Open Drain Mode Control Register 1

ODMCR1 (F789H)

7	6	5	4	3	2	1	0
PWM 10C	PWM00C	P37OC	P24OC	P23OC	P22OC	P21OC	P20OC

(Reset Value 0000 0000)

P37OC	P37 Open Drain Control	0 : Push-pull Output 1 : Open Drain Output	R/W

3.21.5 Port 4 (P47 to P40)

Port 4 is an 8-bit general-purpose I/O port in which each bit can be set independently for input or output using the port 4 control register (P4CR). The port 4 data register (port 4) and port 4 control register (P4CR) are initialized to "0" and set to input mode on a reset.

(1) P40 (DOTXI) and P41 (DOTXO)

P40 and P41 also used as the dot clock oscillator connection pins (DOTXI) and (DOTXO) for the on-screen display circuit (OSD). When P40 and P41 are used as DOTXI and DOTXO, set <DOTXE> of the port 4 mode register (P4MR) to "1".

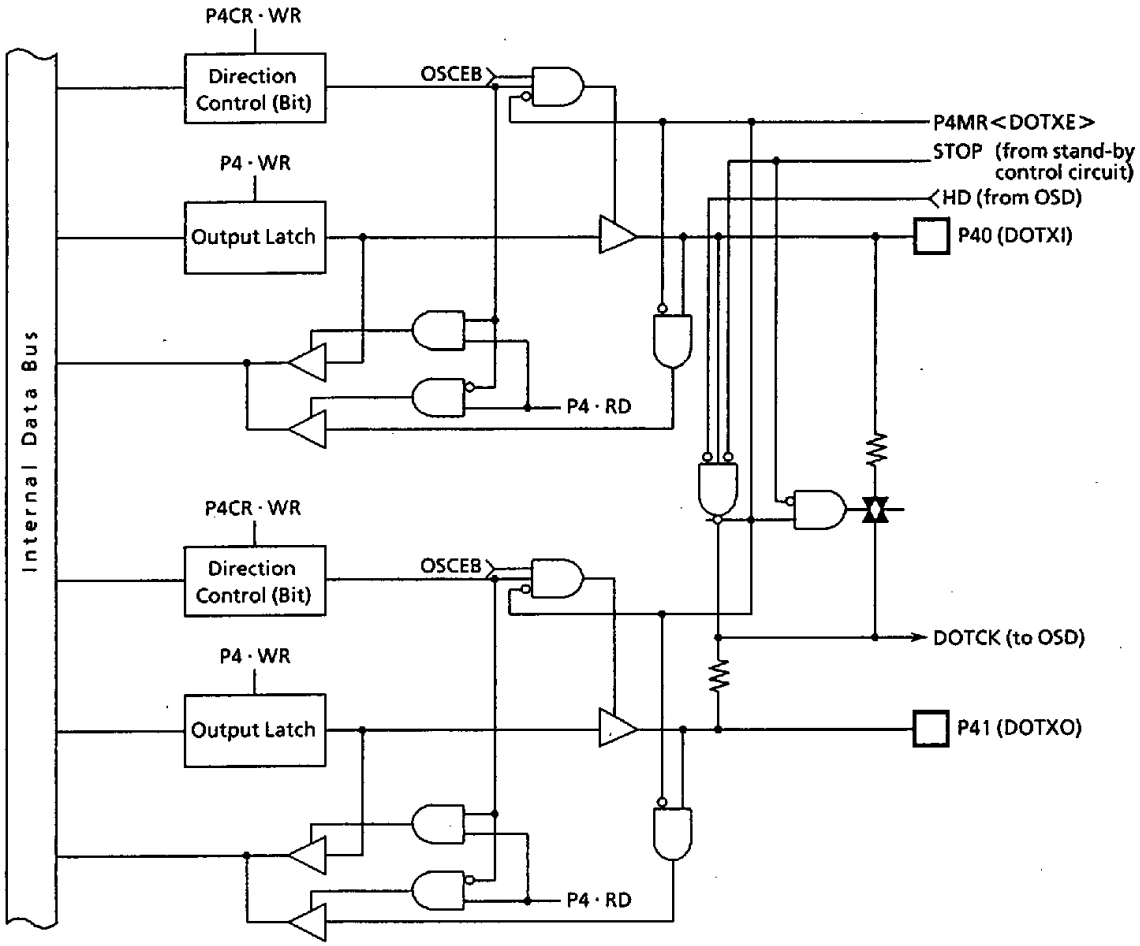


Fig 3.21.15 Port 4 (P41 and P40) Block Diagram

(2) P42 (BLK/TXD1)

P42 also used as the on-screen display (OSD) output blanking signal (BLK) and the serial channel (SIO1) serial data output (TXD1).

When used as BLK or TXD1, set <P42C> of the port 4 control register (P4CR) to "1" to select output mode.

① BLK

The BLK is output by, writing "0" to <P42> of the port 4 data register (port 4), then clearing <TXD1E> of the port 4 mode register (P4MR) to "0", then setting <BLKE> of the P4MR to "1".

② TXD1

To output TXD1, set <TXD1E> of the P4MR to "1".

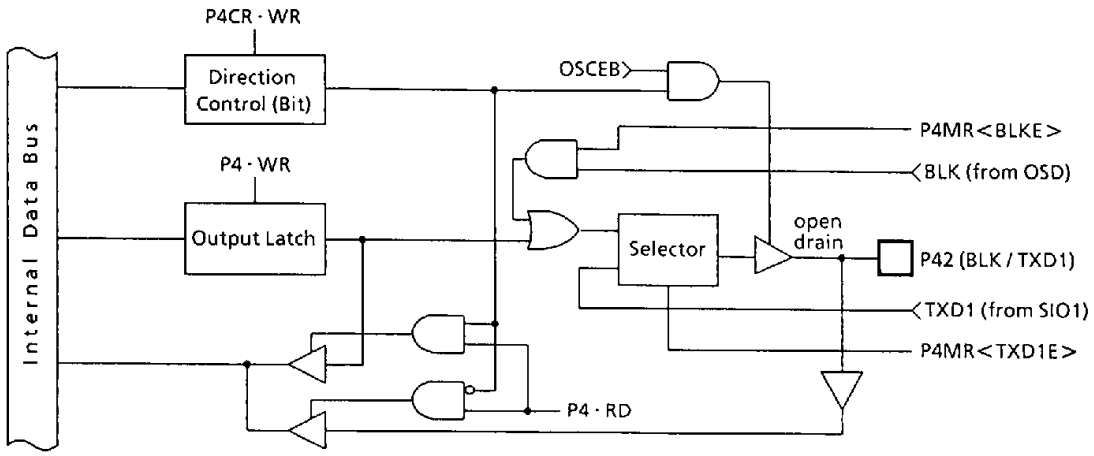


Fig 3.21.16 Port 4 (P42) Block Diagram

(3) P43 (COMPIN)

P43 also used as COMPIN for inputting the signal that results from comparing the SP/EP head FM signals after envelope detection.

When P43 is used as COMPIN, clear <P43C> of the port 4 control register (P4CR) to "0" to select input mode, then set <CRMOD> of the head amp control register (HACR) to "1".

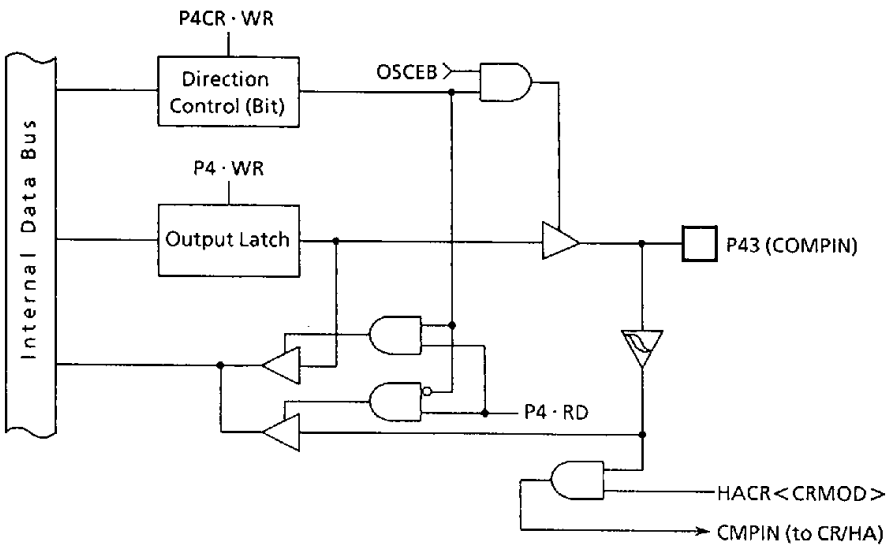


Fig 3.21.17 Port 4 (P43) Block Diagram

(4) P44 (HDIN)

P44 also used as the horizontal sync signal input (HDIN).

When P44 is used as HDIN, clear <P44C> of the port 4 control register (P4CR) to "0" to select input mode.

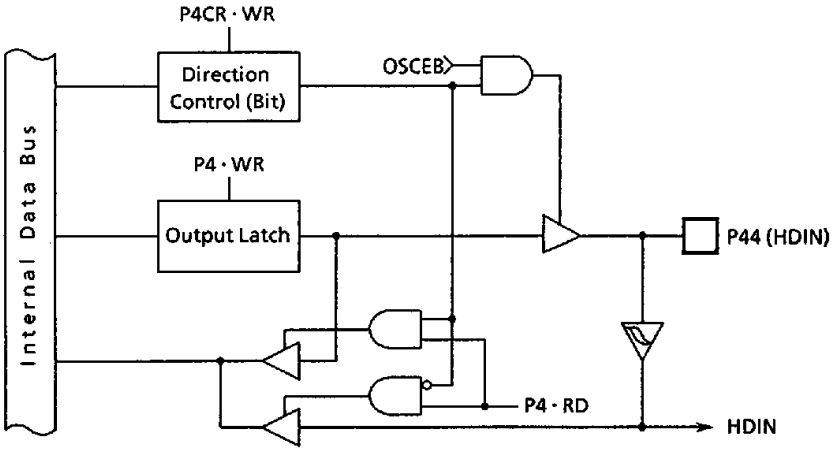


Fig 3.21.18 Port 4 (P44) Block Diagram

(5) P45 (B/RXD1)

P45 also used as the on-screen display (OSD) component video signal (B) output, and also the serial channel (SIO1) serial data input (RXD1).

When P45 is used as B output, set <P45C> of the port 4 control register (P4CR) to "1" to select output mode. The B is output by writing "0" to <P45> of the port 4 data register (port 4), then setting <RGBE> of the port P4 mode register (P4MR) to "1".

When P45 is used as RXD1, clear <P45C> of the P4CR to "0" to select input mode, then set <RXD1E> of the P4MR to "1".

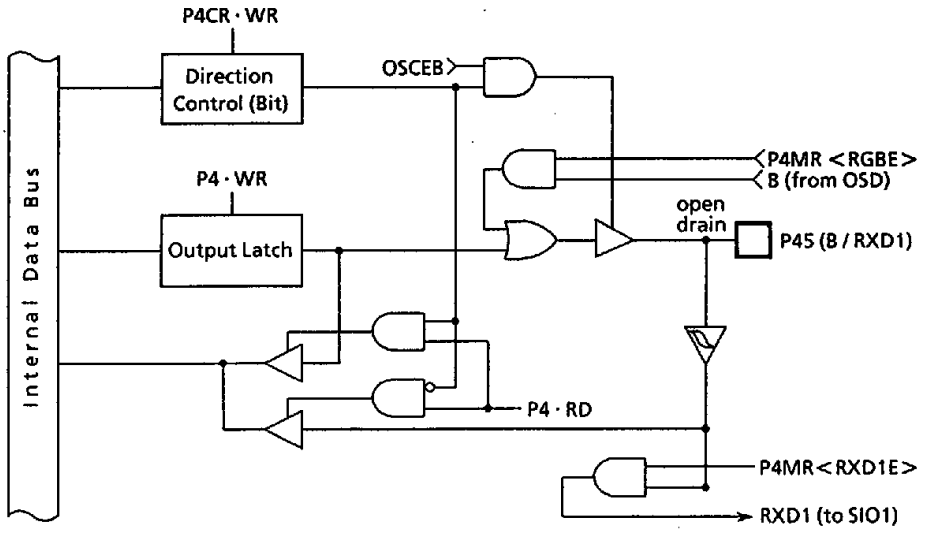


Fig 3.21.19 Port 4 (P45) Block Diagram

(6) P46 (G/SC) and P47 (R/SY)

P46 and P47 also used as the outputs for the component video signals (G and R) for the on-screen display, and the separate color and brightness signals (SC and SY) for the on-screen display.

When P46 is used as G and R, set <P46C, P47C> of the port 4 control register (P4CR) to "1" to select output mode, then write "0" to <P46, P47> of the port 4 data register (port 4). The G and R is output by clearing the <S/N> of the PV control register (PVCR) to "0", then setting <RGBE> of the port 4 mode register (P4MR) to "1".

When P46 is used as SC and SY output, clear <P46C, P47C> of the P4CR to "0", then set <S/N> of the PVCR to "1" to output SC, SY.

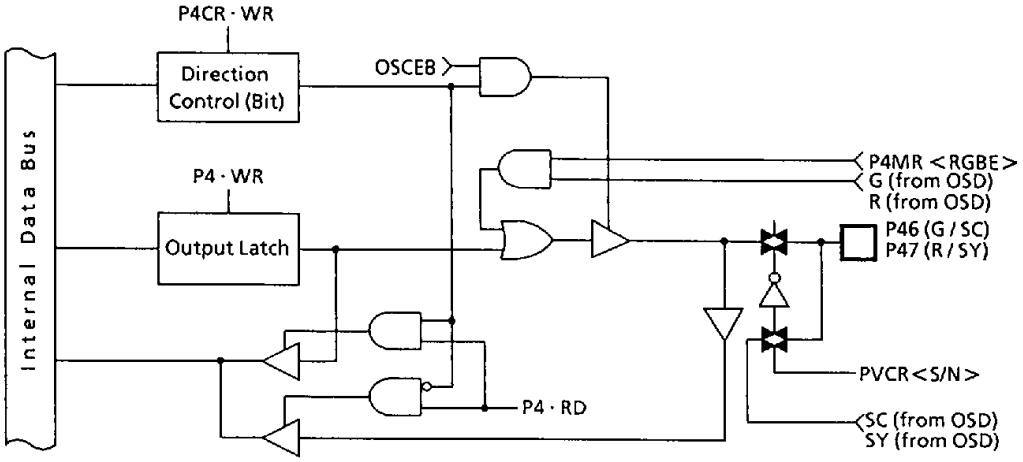


Fig 3.21.20 Port 4 (P46, P47) Block Diagram

Port 4 Data Register

P4 (FFC6H)

7	6	5	4	3	2	1	0
P47	P46	P45	P44	P43	P42	P41	P40

(Reset Value 0000 0000) (R/W)

Port 4 Control Register

P4CR (F784H)

7	6	5	4	3	2	1	0
P47C	P46C	P45C	P44C	P43C	P42C	P41C	P40C

(Reset Value 0000 0000)

P47C to P40C	Port 4 Input/Output control (per bit)	0 : Input 1 : Output	R/W

Port 4 Mode Register

P4MR (F785H)

7	6	5	4	3	2	1	0
$\overline{\text{AFFMIX}}$	SCLK1E	RXD1E	SWPE	BLKE	TXD1E	RGBE	DOTXE

(Reset Value 0000 0000)

RXD1E	RXD1 (P45) input enable/disable	0 : Disabled 1 : Enabled	R/W
BLKE	BLK (P42) output enable/disable	0 : Disabled 1 : Enabled	
TXD1E	TXD1 (P42) output enable/disable	0 : Disabled 1 : Enabled	
RGBE	R (P47), G (P46), B (P45) output enable/disable	0 : Disabled 1 : Enabled	
DOTXE	DOTXI and DOTXO (P40/P41) oscillation enable/disable	0 : Disabled 1 : Enabled	

Head Amp Control Register

HACR (F794H)

7	6	5	4	3	2	1	0
CRMOD	"0"	VTPE34	DFFP01	DFFP00	COMP SEL	CRP0	HAP0

(Reset Value 0000 0000)

CRMOD	CR (P22) output, HA (P23) output, COMPIN (P43) input enable/disable	0 : Disabled 1 : Enabled	R/W

Note : Always write "0" in bit 6 of the Head Amp control register (HACR).

PV Control Register 1

PVCR (F799H)

7	6	5	4	3	2	1	0
XOON	S/N	"0"	MIXOFF	PVSEL3	PVSEL2	PVSEL1	PVSEL0

(Reset Value 0000 0000)

S/N	SC (P46), SY (P47) output enable/disable	0 : Disabled 1 : Enabled	R/W

Note : Always write "0" in bit 5 of the PV control register (PVCR).

3.21.6 Port 5 (P57 to P50)

Port 5 is an 8-bit general-purpose I/O port which can specify input/Output in bit unit. The control register (P5CR) is used to set input/output.

Reset operations clear P5 port data register (P5) and P5 port control register (P5CR) to "0" and initialized to the input mode.

(1) P50 (INT0) and P51 (INT1)

P50 and P51 also used as the external interrupt inputs (INT0 and INT1).

When P50 is used as INT0 and INT1 clear <P50C, P51C> of the port 5 mode control register (P5CR) to "0" to select input mode. <INTE0, INTE1> of the port 5 mode register (P5MR) select the rising or falling edge of INT0 and INT1.

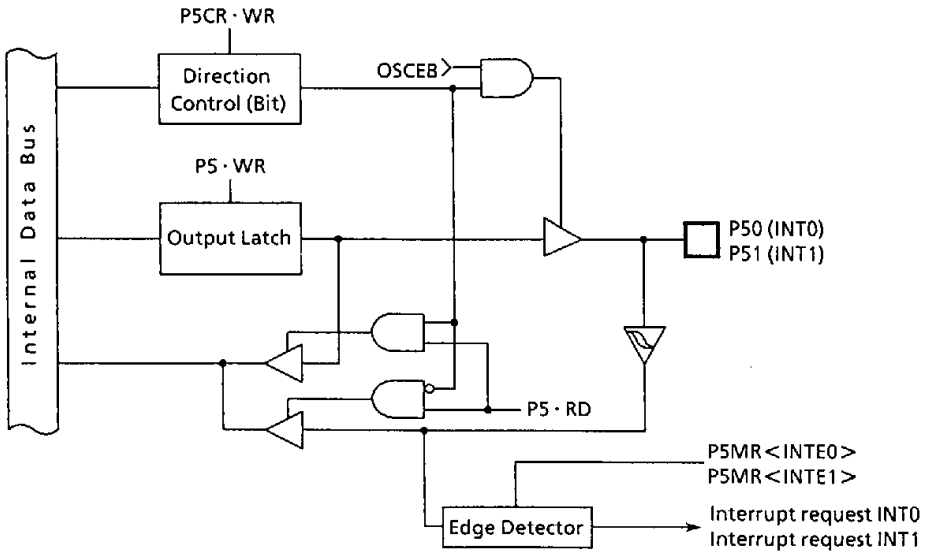


Fig 3.21.21 Port 5 (P51 and P50) Block Diagram

(2) P52 (SDA0/RXD2/VTP0)

P52 also used as the serial bus interface (SBI) I2C bus mode serial bus data I/O (SDA0), the SIO mode serial data input (RXD2), and pulse output VTP0.

When P52 is used as SDA0 I/O and VTP0, set <P52C> of the port 5 control register (P5CR) to "1" to select output mode.

When P52 is used as RXD2, clear <P52C> of the P5CR to "0" to select input mode.

The output circuit format can be set to push-pull output or N-channel open drain output by <P52OC> in the open drain control register 2 (ODMCR2).

① SDA0

Write "1" to <P52> of the port 5 data register (port 5), then set <P52OC> of the ODMCR2 to "1" for open drain output.

② RXD2

③ VTP0

The data written to <VTP0D> of the TP data register (TPDR) can be output in sync with the rising or falling edge of TPG03 in the timing pulse generator 0 (TPG0) output.

When P52 is used as VTP0, set <VTP0E> of the port 5 mode register (P5MR) to "1", then set <VTPE0> of the P5MR for TPG03 edge selection.

(3) P53 (SCL0 / SCLK2 / VTP1)

P53 also used as the serial bus interface (SBI) I2C bus mode serial clock I/O (SCL0), or the SIO mode serial clock I/O (SCLK2), and also pulse output VTP1.

When P53 is used as SCL0 I/O, SCLK2 output, and VTP1, set <P53C> of the port 5 control register (P5CR) to "1" to select output mode.

When P53 is used as SCLK2, clear <P53C> of the P5CR to "0" to select input mode.

The output circuit format can be set to push-pull output or N-channel open drain output by <P53OC> in the open drain control register 2 (ODMCR2).

① SCL0

Write "1" to <P53> of the port 5 data register (port 5), then set <P53OC> of the ODMCR2 to "1" for open drain output.

② SCLK2

③ VTP1

The data written to <VTP1D> of the TP data register (TPDR) can be output in sync with the rising or falling edge of output TPG03 in the timing pulse generator 0 (TPG0).

When P53 is used as VTP1, set <VTP1E> of the port 5 mode register (P5MR) to "1", then set <VTPE1> of the P5MR for TPG03 edge selection.

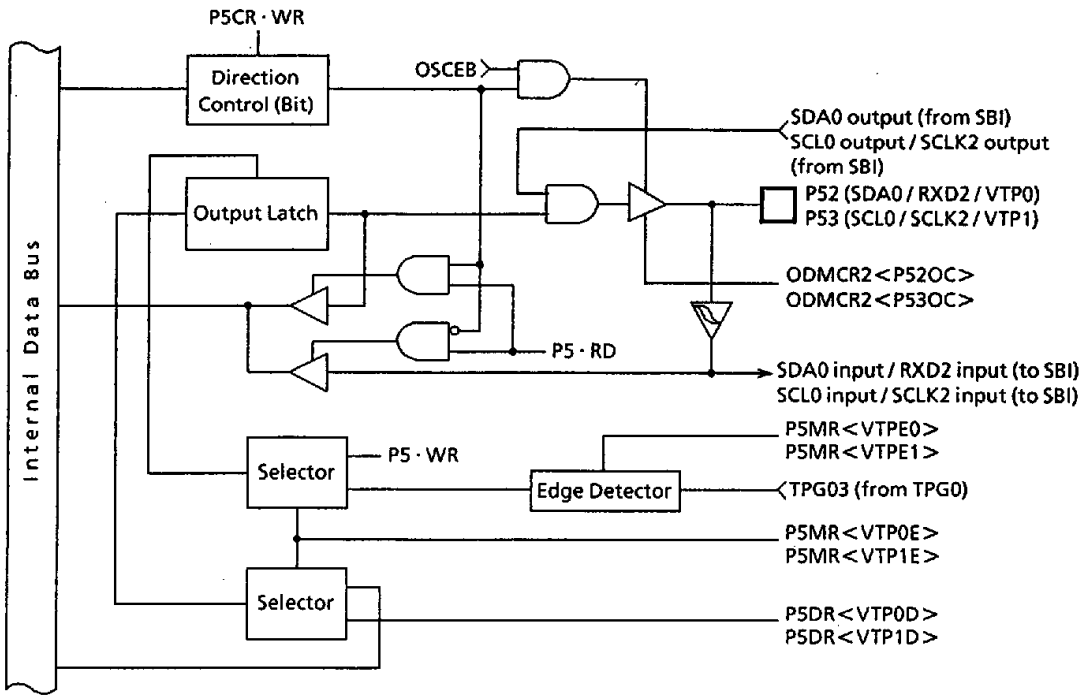


Fig 3.21.22 Port 5 (P52 and P53) Block Diagram

(4) P54 (TXD2/VTP2)

P54 also used as the serial bus interface (SBI) SIO mode serial data output (TXD2) and also pulse output VTP2.

When P54 is used as TXD2 and VTP2, set <P54C> of the P5CR to "1" to select output mode.

① TXD2

Write "1" to <P54> of the port 5 data register (P5).

② VTP2

The data written to <VTP2D> of the TP data register (TPDR) can be output in sync with the rising or falling edge of TPG03 in the timing pulse generator 0 (TPG0) output.

When P54 is used as VTP2, set <VTP2E> of the port 5 mode register (P5MR) to "1", then setting <VTPE2> of the P5MR for TPG03 edge selection.

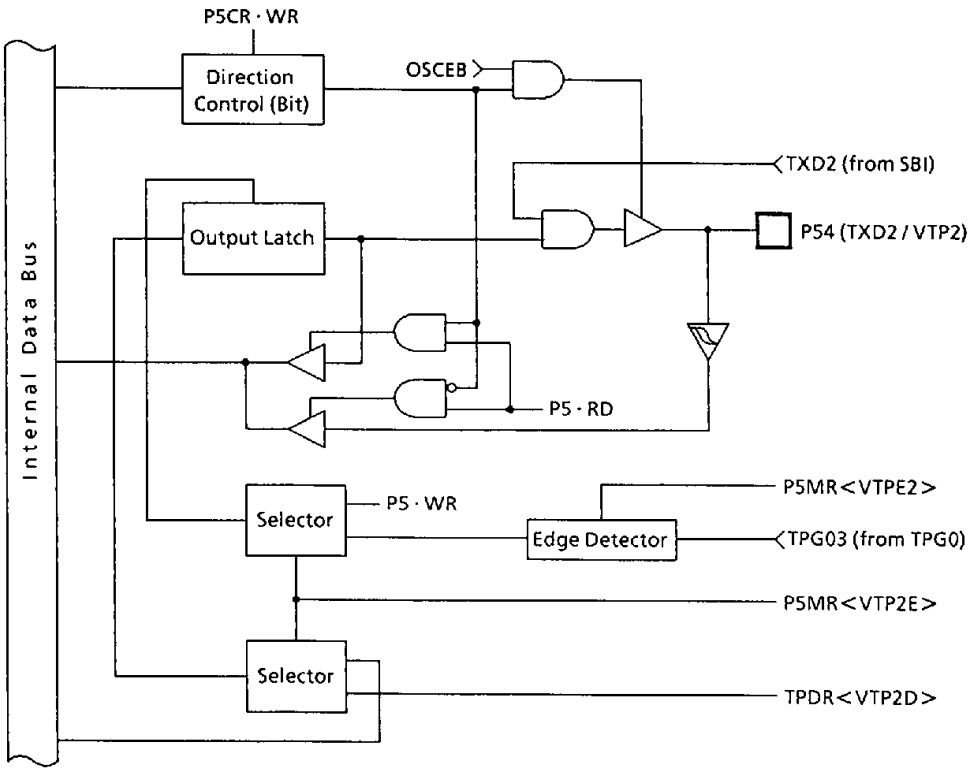


Fig 3.21.23 Port 5 (P54) Block Diagram

(5) P55 (SDA1), and P56 (SCL1)

P55 also used as the serial bus interface (SBI) I2C bus mode serial bus data I/O (SDA1), and also P56 functions as the I2C bus mode serial clock I/O (SCL1).

When P55 and P56 are used as SDA1 I/O and SCL1 I/O, write "1" to <P55> and <P56> of the port 5 data register (port 5), then set <P55C, P56C> of the port 5 control register (P5CR) to "1" to select output mode. Also set <P55OC, P56OC> of the open drain control register 2 (ODMCR2) to "1" to select open drain output.

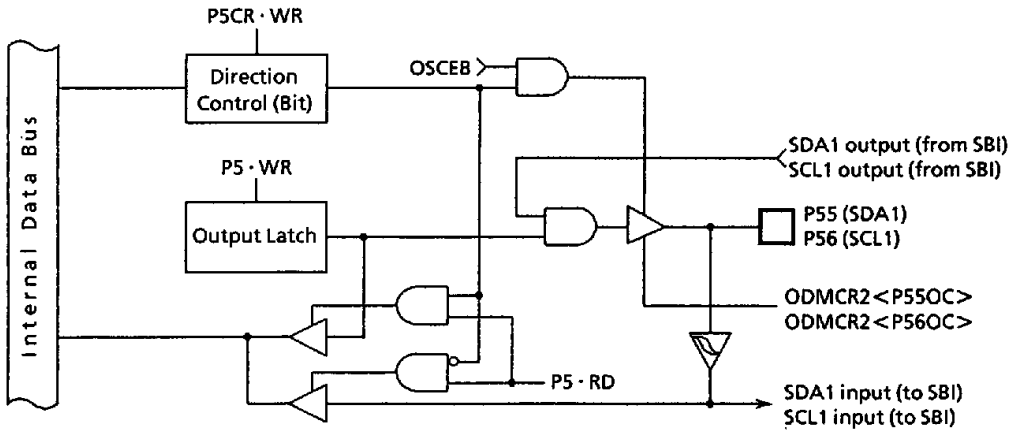


Fig 3.21.22 Port 5 (P55 and P56) Block Diagram

(6) P57 (SCLK1)

P57 also used as the serial channel (SIO1) serial clock I/O (SCLK1).

When P57 is used as serial clock output, set <P57C> of the port 5 control register (P5CR) to "1" to select output mode, then set <SCLK1E> of the port 4 mode register (P4MR) to "1".

When P57 is used as serial clock input, clear <P57C> of the P5CR to "0" to select input mode.

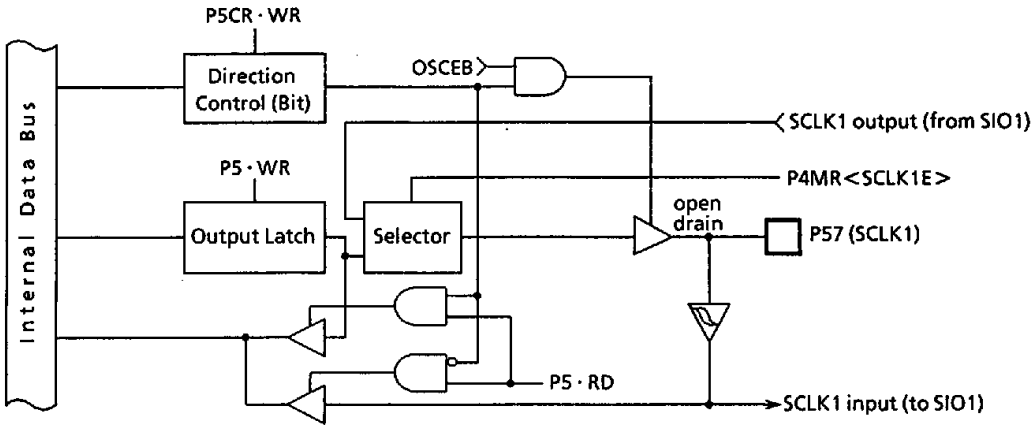


Fig 3.21.23 Port 5 (P57) Block Diagram

Port 5 Data Register

P5 (FFC7H)

7	6	5	4	3	2	1	0
P57	P56	P55	P54	P53	P52	P51	P50

(Reset Value 0000 0000) (R/W)

Port 5 Control Register

P5CR (F786H)

7	6	5	4	3	2	1	0
P57C	P56C	P55C	P54C	P53C	P52C	P51C	P50C

(Reset Value 0000 0000)

P57C to P50C	Port 5 Input /Output control (per bit)	0 : Input 1 : Output	R/W

Port 5 Mode Register

P5MR (F787H)

7	6	5	4	3	2	1	0
VTPE2	VTPE1	VTPE0	VTP2E	VTP1E	VTP0E	INTE1	INTE0

(Reset Value 0000 0000)

VTPE2	VTP2 (P54) Trigger Edge Selection	0 : Rising 1 : Falling	R/W
VTPE1	VTP1 (P53) Trigger Edge Selection	0 : Rising 1 : Falling	
VTPE0	VTP0 (P52) Trigger Edge Selection	0 : Rising 1 : Falling	
VTP2E	VTP2 output enable/disable	0 : Disabled 1 : Enabled	
VTP1E	VTP1 output enable/disable	0 : Disabled 1 : Enabled	
VTP0E	VTP0 output enable/disable	0 : Disabled 1 : Enabled	
INTE1	INT1 (P51) Interrupt Edge Selection	0 : Rising 1 : Falling	
INTE0	INT2 (P50) Interrupt Edge Selection	0 : Rising 1 : Falling	

Port 4 Mode Register

P4MR (F785H)

7	6	5	4	3	2	1	0
AFFMIX	SCLK1E	RXD1E	SWPE	BLKE	TXD1E	RGBE	DOTXE

(Reset Value 0000 0000)

SCLK1E	SCLK1 (P57) output enable/disable	0 : Disabled 1 : Enabled	R/W

TP Data Register

TPDR (FFDBH)

7	6	5	4	3	2	1	0
VTP3D	VTP2D	VTP1D	VTP0D	TP3D	TP2D	TP1D	TP0D

(Reset Value 0000 0000)

VTP2D	VTP2 (P54) Data Register		R/W
VTP1D	VTP1 (P53) Data Register		
VTP0D	VTP0 (P52) Data Register		

Open Drain Mode Control Register 2

ODMCR2 (F78AH)

7	6	5	4	3	2	1	0
			P74OC	P56OC	P55OC	P53OC	P52OC

(Reset Value ***0 0000)

P56OC	Open drain control of P56/P55/P53/P52 output	0 : Push-pull output 1 : Open drain output	R/W
P55OC			
P53OC			
P52OC			

3.21.7 Port 6 (P67 to P60)

Port 6 is an 8-bit general-purpose input port and also functions as the 8-bit A/D conversion (A/D) input pins (AIN0 to AIN7). The port 6 data register (port 6) is not initialized on a reset.

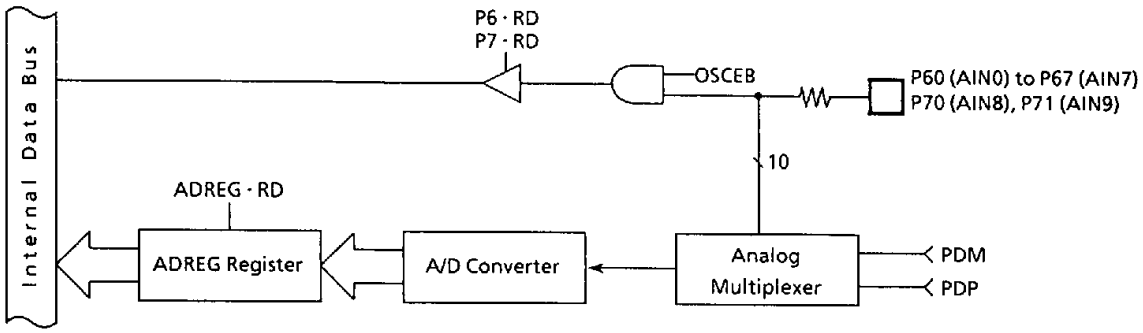


Fig 3.21.26 Port 6 (P67 to P60), Port 7 (P71 and P70) Block Diagram

Port 6 Data Register

P6 (FFC8H)	7	6	5	4	3	2	1	0	(Reset Value **** ****)	Read only
	P67	P66	P65	P64	P63	P62	P61	P60		

3.21.8 Port 7 (P74 to P70)

Port 7 is an 5-bit general-purpose I/O port.P70 and P71 are input ports, and P72 and P73 can specify input/Output in bit unit. P74 is output port. The control register (P7CR) is used to set input/output.
Reset operations clear except for P70 and P71, P7 port data register (P1) and P1 port control register (P1CR) to "0" and initialized to the input mode.

(1) P70 (AIN8) and P71 (AIN9)

P70 and P71 also used as an 8-bit A/D converter (A/D) input pin (AIN8 and AIN9).
<P70 and P71> in Port 7 control register are not initialized by resetting operation.
See Figure 3.21.6, "port 6 (P60 to P67) and port 7 (P70 and P71) block diagram" for details of the block diagram of P70 and P71.

(2) P72 (XTIN) and P73 (XTOUT)

P72 and P73 also used as low-frequency oscillator connection pin (XTIN and XTOUT).
When P72 and P73 are used as XTIN and XTOUT, set <XTEN> in system control register 1 (SYSCR1) to "1" to stat ocillation.

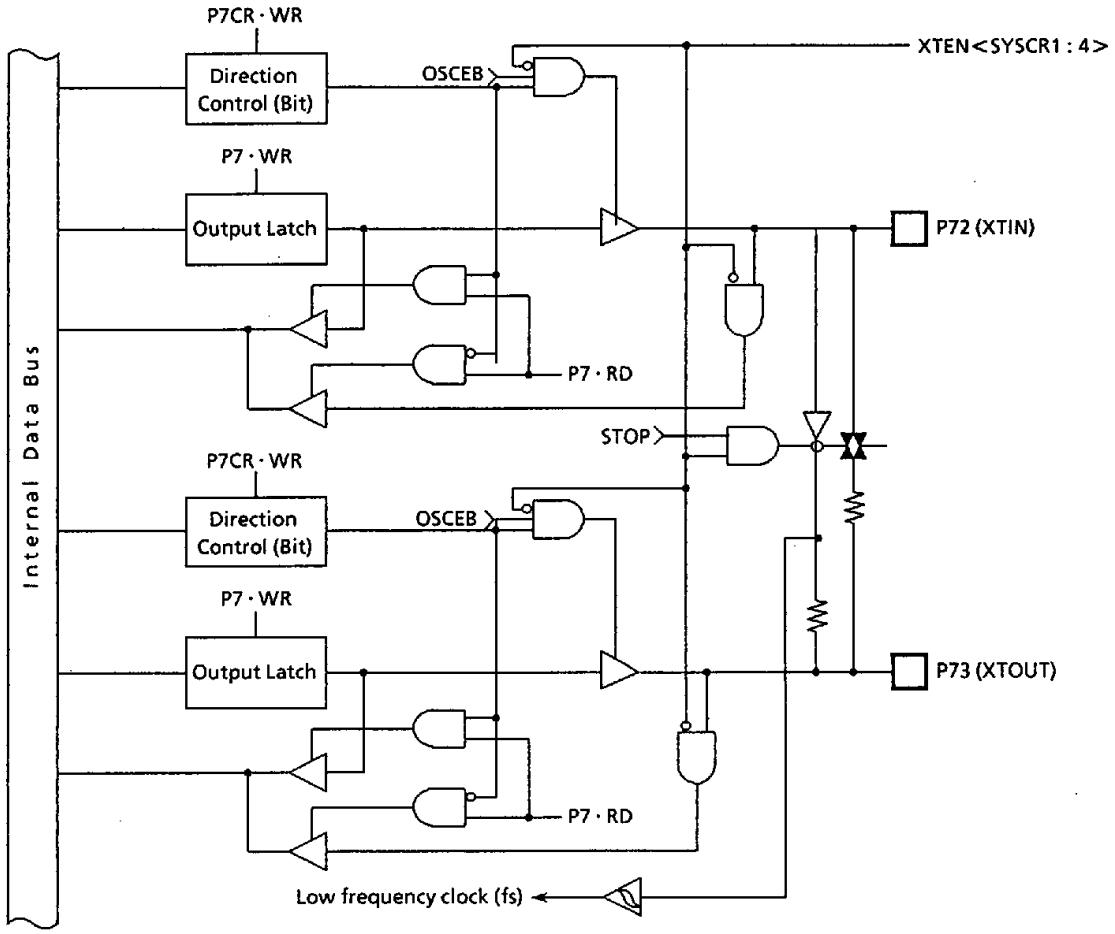


Fig 3.21.27 Port 7 (P73 and P72) Block Diagram

(3) P74 (PWM2/PWM3)

P74 used as an 8-bit pulse width moduration output(PWM2) and also 14-bit pulse width moduration output (PWM3).

When used as PWM2 and PWM3, set <P74M> Port 7 control register (P7CR) to "1".

PWM2 and PWM3 are output by setting <PWM2RUN and PWM3RUN) in the timer start control register (TRUN) to "1".

Selection of PWM2 or PWM3 can be set to <PWMSEL> in the PWM control register (PWMCR). And the polarity of PWM output inverte by setting <PWMP02> in PWMCR.

The output circuit format can be set to push-pull output or N-channel open drain outputby setting <P74OC> in open drain control register2 (ODMCR2).

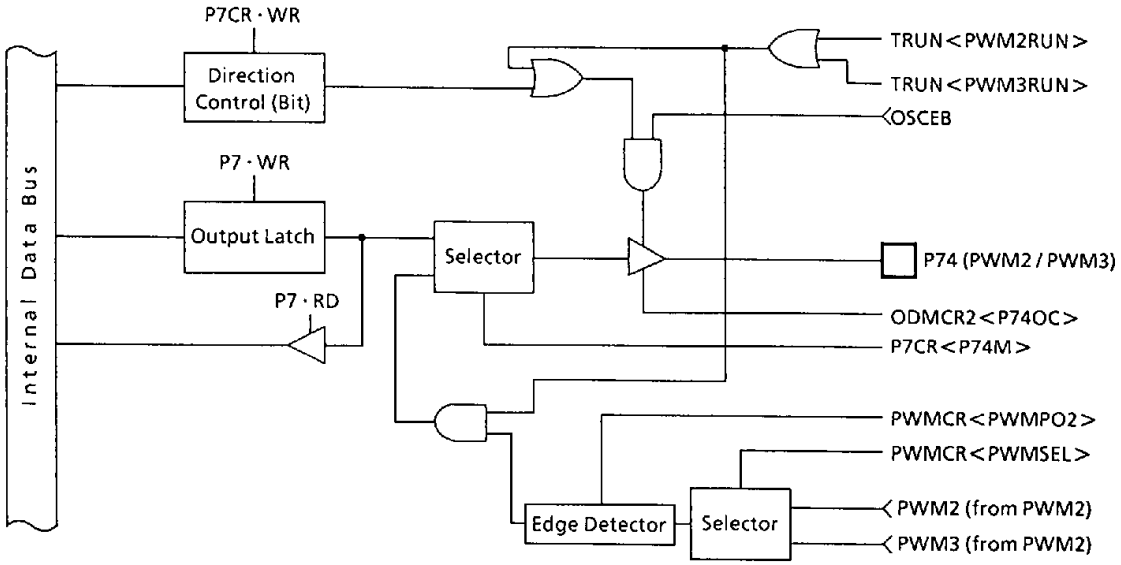


Fig. 3.21.28 Port 7 (P74) Block Diagram

Port 7 Data Register

P7 (FFC9H)

7	6	5	4	3	2	1	0
		VTP4D	P74	P73	P72	P71	P70

(Reset Value **00 00**) (R/W)

Note) P71 and P70 are read only.

Port 7 Control Register

P7CR (F788H)

7	6	5	4	3	2	1	0
		P74M	P74C	P73C	P72C		

(Reset Value **00 00**)

P74M	PWM2/PWM3 (P74) output enable/disable	0 : Disabled 1 : Enabled	R/W
P74C to P72C	P74 to P72 I/O control (per bit)	0 : Input mode 1 : Output mode	

PWM Control Register

PWMCR (F793H)

7	6	5	4	3	2	1	0
	PWM12 MOD	CFR TRGS	CSYN CP0	PWM SEL	PWMP02	PWMP01	PWMP00

(Reset Value *000 0000)

PWMSEL	PWM output (P74) Selection	0 : PWM2 1 : PWM3	R/W
PWMPO2	PWM2 / PWM3 (P74) Output Polarity Switch	0 : Positive (+) 1 : Inverted	

Timer Start Control Register

TRUN (F793H)

7	6	5	4	3	2	1	0
PWM3 RUN	T3RUN	PWM1 RUN	PWM0 RUN	PWM2 RUN	T2RUN	T1RUN	T0RUN

(Reset Value 0000 0000)

PWM3RUN	PWM3 start/stop	0 : Stop 1 : Start	R/W
PWM2RUN	PWM2 start/stop	0 : Stop 1 : Start	

Open Drain Mode Control Register 2

ODMCR2 (F78AH)

7	6	5	4	3	2	1	0
			P74OC	P56OC	P55OC	P53OC	P52OC

(Reset Value ***0 0000)

P74OC	P74 open drain control	0 : Push-pull output 1 : Open Drain output	R/W

3.21.9 Port 8 (P81 to P80)

Port 8 is a 2-bit general-purpose output port. The port 8 data register (P8) is reset to "0" on a reset.

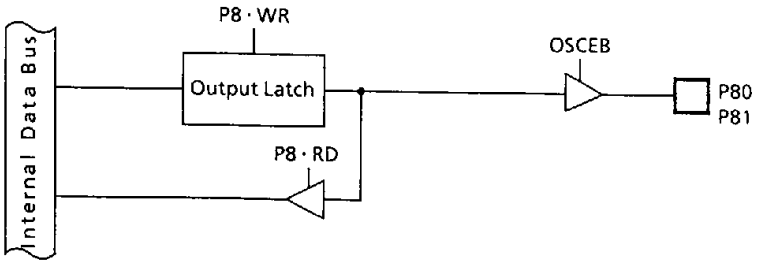


Fig 3.21.29 Port 8 Block Diagram

Port 8 Data Register

P8 (FFB4H)	7	6	5	4	3	2	1	0
							P81	P80

(Reset Value **** **00)

3.21.10 Special Function PORT

(1) Pulse width modulation output (PWM0 and PWM1)
This port is dedicated to 12-bit PWM (PWM0 and PWM1) output.
See 3.11.1, "12-bit PWM (PWM0 and PWM1)" for details.

(2) Head switching signal output (VASWP)
The timing pulse generator 0 (TPG0) output, TPG03, can be used as the cylinder head switching signal (DFF), which can be output from the VASWP pin.
See 3.13, "Head Amp/Color Rotary Control Circuit" for details.

(3) OSD oscillator connection pins (XI/XO)
These are the main clock oscillation circuit for the on-screen display (OSD) circuit and are used to connect an oscillator that provides a frequency four times that of the fsc (color subcarrier frequency).
Setting <XOON> of the PV control register (PVCR) to "1" enables the oscillation circuit.

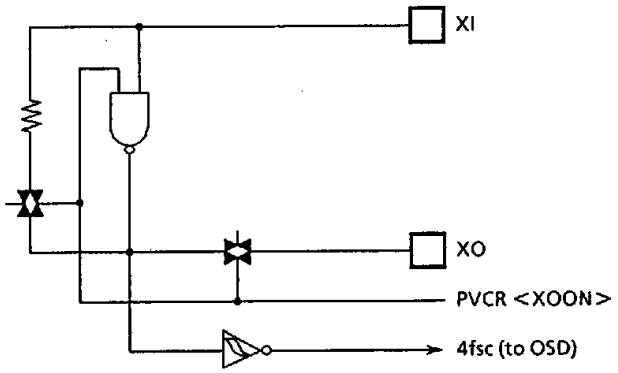


Fig 3.21.30 Structure of OSD Oscillator Circuit (XI/XO)

PV Control Register

PVCR (F799H)	7	6	5	4	3	2	1	0	(Reset Value 0000 0000)
	XOON	S/N	"0"	$\overline{\text{BLKMIX}}$	HPMIX	PVSEL2	PVSEL1	PVSEL0	

XOON	OSD oscillation (XI/XO) and vertical sync input (VDIN) enable/disable	0 : Disabled 1 : Enabled	R/W

Note: Always write "0" to bit 5 of the PV control register (PVCR).

(4) Vertical Sync Signal Input (VDIN)

This port is used only for the external input of the vertical sync signal of the on-screen display (OSD) circuit. Input is enabled by setting <XOON> of the PV control register (PVCR) to "1".

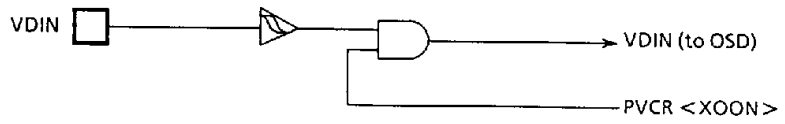


Fig 3.21.31 Structure of Vertical Sync Signal Input (VDIN)

PV Control Register

PVCR (F799H)	7	6	5	4	3	2	1	0	(Reset Value 0000 0000)
	XOON	S/N	"0"	$\overline{\text{BLKMIX}}$	HPMIX	PVSEL2	PVSEL1	PVSEL0	

XOON	OSD oscillation (XI/XO) and vertical sync input (VDIN) enable/disable	0 : Disabled 1 : Enabled	R/W

Note: Always write "0" in bit 5 of the PV control register (PVCR).

(5) Composite Sync Signal Input (CSYN)

This is the input for the composite sync signal. The sync signal separation circuit (CSYNC) separates the vertical sync signal (V.SYNC) from the horizontal sync signal (H.SYNC).

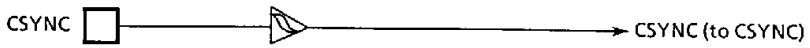


Fig 3.21.32 Structure of Composite Sync Signal Input (CSYNC)

(6) Clock Output (CLK)

The base clock (high-frequency clock fc or low-frequency clock fs) can be output from CLK divided by 4 or divided by 2.

<CLKCK> of the interrupt control register (INTCR) selects the division ratio of CLK. <CLOE> of the INTCR enables and disables CLK output.

The CLK pin is pulled up to H level by a reset.

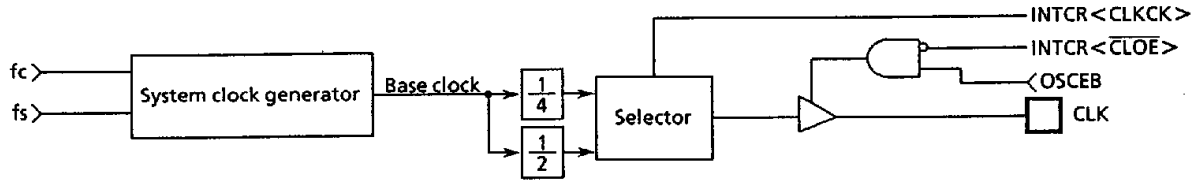


Fig 3.21.32 Structure of Clock Output (CLK)

Interrupt Control Register

INTCR (F78FH)

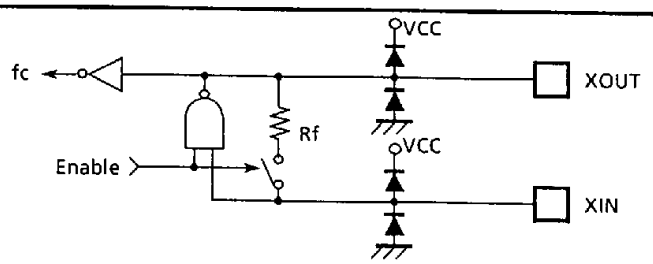
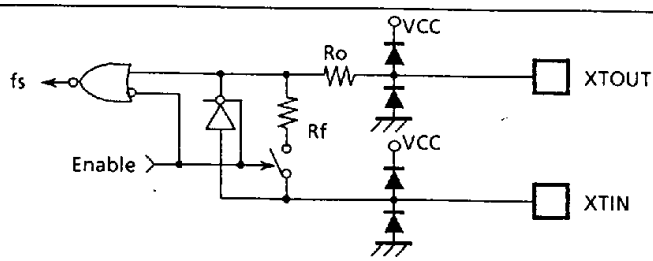
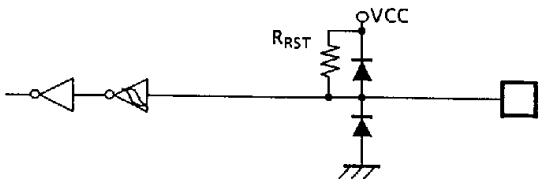
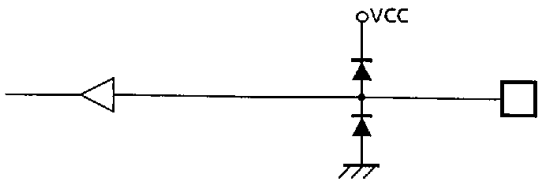
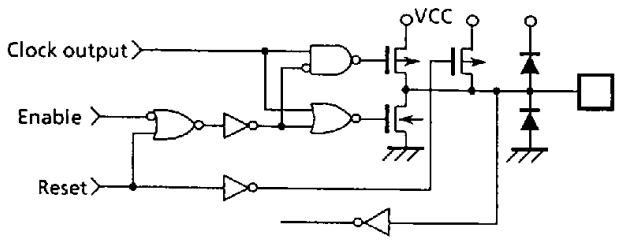
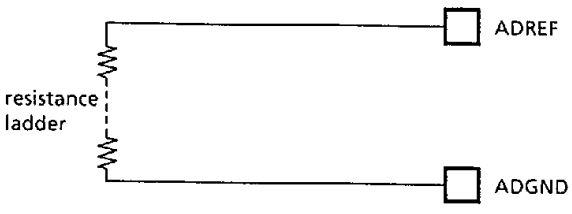
7	6	5	4	3	2	1	0
		CLKCK	CLOE	INTT PG0E	INTT PG0S	T3ADS	T0DIRS

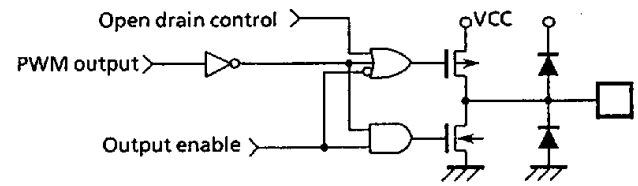
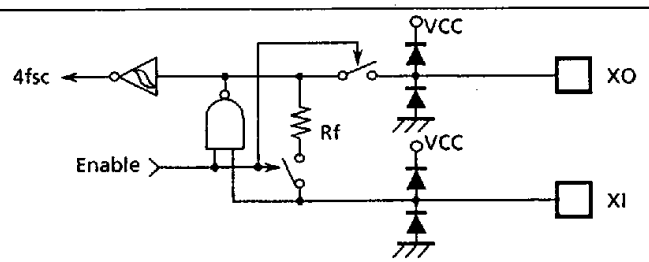
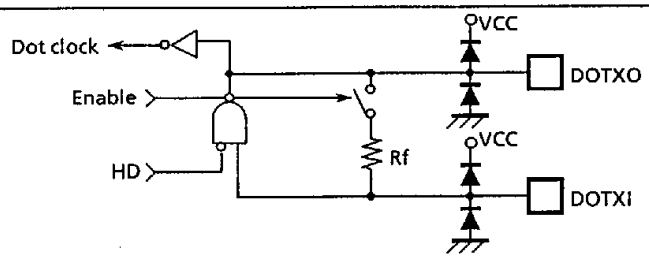
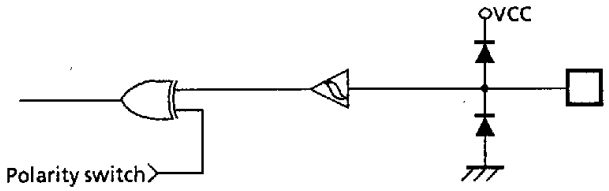
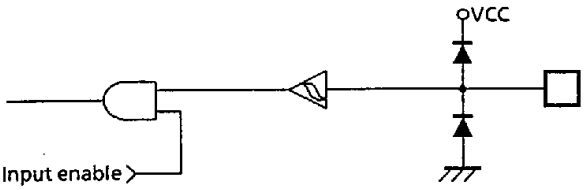
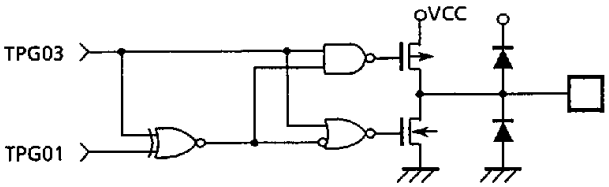
(Initial value **00 0000)

CLKCK	CLK output frequency selection	0 : fc/4 or fs/4 1 : fc/2 or fs/2	R/W
CLOE	CLK output enable/disable	0 : Enabled 1 : Disabled	

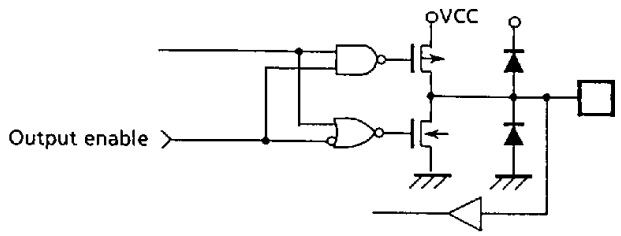
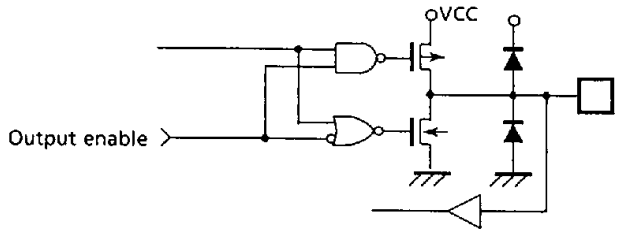
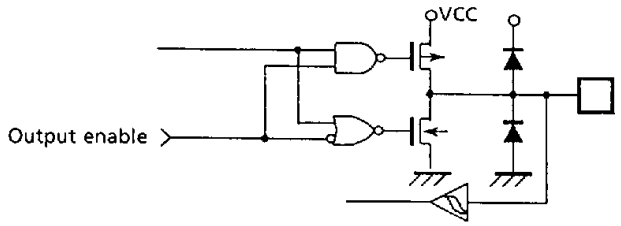
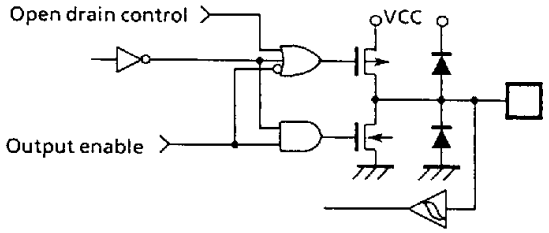
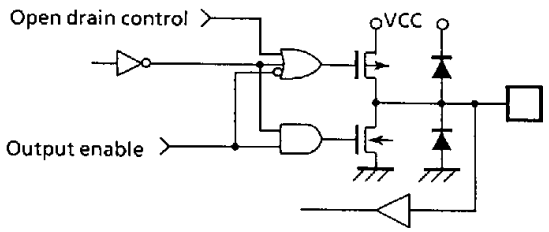
4. PINS OF INPUT / OUTPUT CIRCUIT

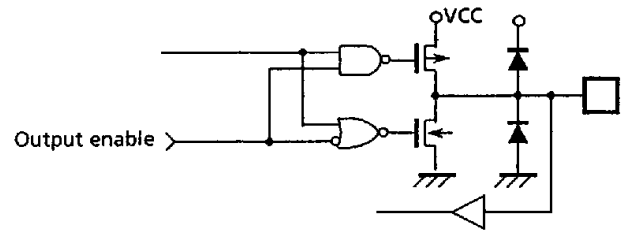
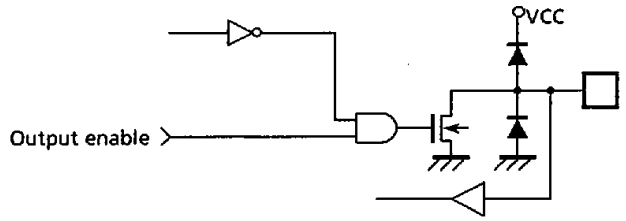
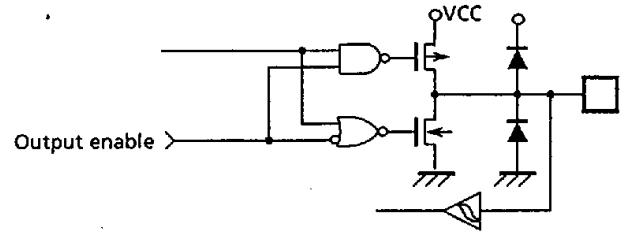
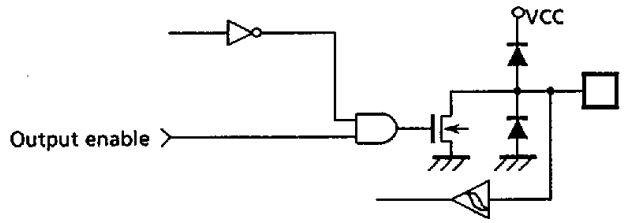
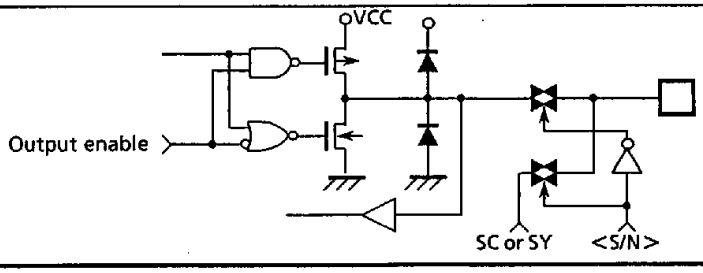
(1) Control pin

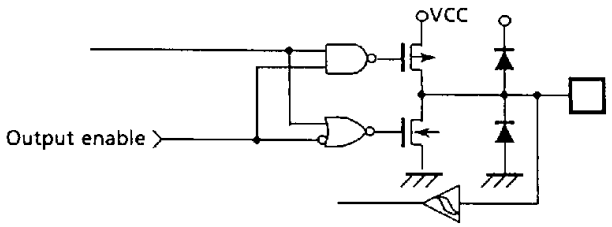
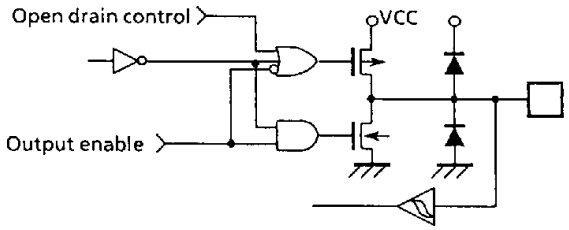
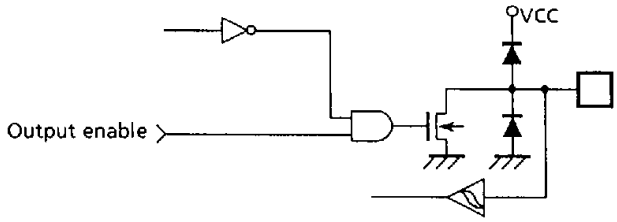
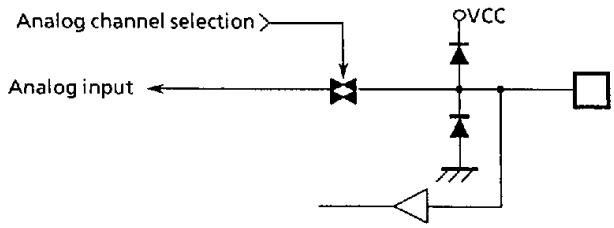
CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
XIN XOUT	Input / Output		Resonator connecting pins (high-frequency) Rf = 1.2 MΩ (Typ.)
XTIN XTOUT	Input / Output		Also used as resonator connecting pins (low-frequency), P72 and P73 Rf = 6 MΩ (Typ.) Ro = 220 kΩ (Typ.)
$\overline{\text{RESET}}$	Input		Schmit input Pull-up resistor R_{RST} = 100 kΩ (Typ.)
$\overline{\text{TEST}}$	Input		Final test pin Fix to "H" level
CLK	Output		
ADREF ADGND			Analog reference voltage pin I_{REF} = 0.6 mA (Typ.)

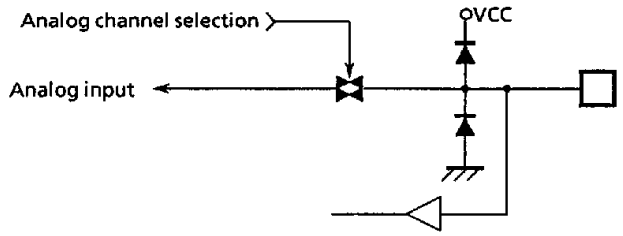
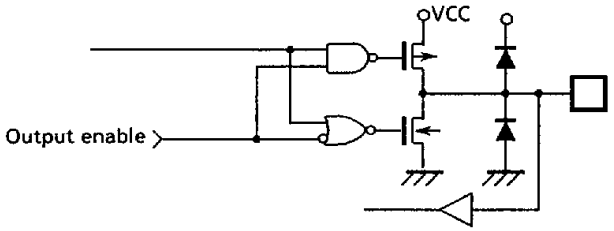
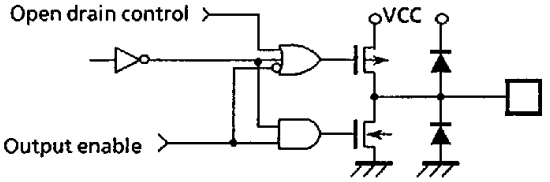
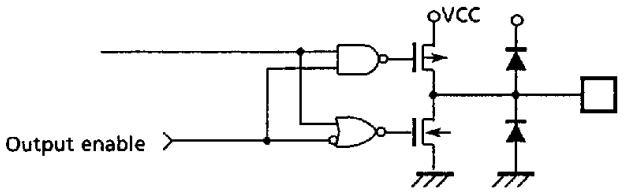
CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
PWM0 PWM1	Output		Tri-start output Open drain output (Programmable)
XI XO	Input / Output		OSD oscillator connecting pins Rf = 1.2 MΩ (Typ.)
DOTXI DOTXO	Input / Output		Also used as oscillator connecting pins, P40 and P41 Rf = 1.2 MΩ (Typ.)
CSYNC	Input		CSYNC input Schmit input
VDIN	Input		OSD VD input Schmit input
VASWP	Output		Head switch signal output Tri-state output

(2) I/O port

CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
P0 P1	Input / Output		Tri-state I/O
P2 P3	Input / Output		Tri-state I/O P26, P30
	Input / Output		Tri-state I/O Schmit input P25, P27 P31 to P36
	Input / Output		Tri-state I/O Open drain output (programmable) Schmit input P24
	Input / Output		Tri-state I/O Open drain output (programmable) P20 to P23 P37

CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
P4	Input / Output		Tri-state I/O P40, P41
	Input / Output		Open drain output P42
	Input / Output		Tri-state I/O Schmit input P43, P44
	Input / Output		Open drain output Schmit input P45
	Input / Output		Tri-state I/O P46, P47

CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
P5	Input / Output		Tri-state I/O Schmit input P50, P51, P54
	Input / Output		Tri-state I/O Open drain output (Programmable) Schmit input P52, P53, P55, P56
	Input / Output		Open drain output Schmit input P57
P6	Input		

CONTROL PIN	I/O	INPUT/OUTPUT CIRCUIT	REMARKS
P7	Input		P70, P71
	Input / Output		Also used as Tri-state output, XTIN and XTOUT P72, P73
	Output		Tri-state output Open drain output (programmable) P74
P8	Output		Tri-state output P80, P81

5. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS (or note)	RATING	UNIT
Supply voltage	V_{CC}	DVCC1, DVCC2, AVCC1, AVCC2	− 0.5 to + 6.5	V
Input voltage	V_{IN}		− 0.5 to V_{CC} + 0.5	V
Output Voltage	V_{OUT1}		− 0.5 to V_{CC} + 0.5	V
Output Current (Per 1 pin)	I_{OUT1}	Analog Output pin (Source Current)	− 10	mA
	I_{OUT2}	Digital Output pin (Source Current)	− 3.2	mA
	I_{OUT3}	Analog Output pin (Sink Current)	10	mA
	I_{OUT4}	Digital Output pin (Sink Current)	3.2	mA
Output Current (Total)	ΣI_M	$\Sigma I_M = \Sigma I_{OUT1} + \Sigma I_{OUT2}$	− 50	mA
	ΣI_P	$\Sigma I_P = \Sigma I_{OUT3} + \Sigma I_{OUT4}$	100	mA
Power Dissipation (Ta = 70°C)	P_D		700	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		− 65 to + 150	°C
Operating Temperature	Topr		− 20 to + 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, Topr = − 20 to + 70 °C)

PARAMETER		CONDITION	SYMBOL	Min.	Max.	UNIT
Supply voltage		NORMAL mode IDLE mode	V_{CC}	4.5	5.5	V
		SLOW mode SLEEP mode		2.7		
Input High Voltage	Except of hysteresis input	Vcc ≧ 4.5 V	V_{IH1}	V_{CC} × 0.70	V_{CC}	V
	Hysteresis input pin	Vcc ≧ 4.5 V	V_{IH2}	V_{CC} × 0.75		
	All of degital input pin	Vcc < 4.5 V	V_{IH3}	V_{CC} × 0.90		
Input Low Voltage	Except of hysteresis input	Vcc ≧ 4.5 V	V_{IL1}	0	V_{CC} × 0.30	V
	Hysteresis input pin	Vcc ≧ 4.5 V	V_{IL2}		V_{CC} × 0.25	
	All of degital input pin	Vcc < 4.5 V	V_{IL3}		V_{CC} × 0.10	
Clock Frequency	XIN / XOUT pin		fc	−	16.0	MHz
	XTIN / XTOUT pin		fs	30.0	34.0	kHz

D.C. Characteristics (Topr = – 20 to + 70 °C)

PARAMETER		CONDITION	SYMBOL	Min.	Typ.	Max.	UNIT
Digital Current consumption	NORMAL mode	V_{CC} = 5.5 V fc = 16 MHz, fs = 32.8 kHz	I_{CCO1}	–	40	60	mA
	IDLE mode		I_{CCL1}	–	15	25	mA
	SLOW mode	V_{CC} = 3 V fs = 32.8 kHz	I_{CCO2}	–	100	200	μA
	SLEEP mode		I_{CCL2}	–	50	100	μA
	STOP mode	V_{CC} = 5.5 V	I_{CCS}	–	0.5	50	μA
Analog Current consumption	NORMAL mode	$AV_{CC}1 = AV_{CC}2$ = 5.0 V	I_{CCA}	–	25	40	mA
High-level output voltage		V_{CC} = 4.5 V, I_{OH} = – 0.7 mA	V_{OH1}	V_{CC} – 0.4	–		V
High-level output voltage		V_{CC} = 4.5 V, I_{OH} = – 200 μA	V_{OH2}	2.4	–	–	V
Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 1.6 mA	V_{OL1}	–	–	0.4	V
Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 3.0 mA	V_{OL2}	–	–	0.4	V
Hysteresis voltage			V_{HS}	–	0.70	–	V
INPUT Leakage Current		$0V \leqq Vin \leqq V_{CC}$	I_{LI}	–	0.05	± 10	μA
OUTPUT Leakage Current		$0.2V \leqq VOUT \leqq V_{CC} - 0.2V$	I_{LO}	–	0.05	± 10	μA
$\overline{RESET}$ pin Pull-up Current		V_{CC} = 5.5 V, Vin = 0.2 V	I_{RST}	30	–	120	μA

A/D Conversion characteristic (Topr = – 20 to + 70 °C, V_{CC} = 4.5 to 5.5 V, fc = 16 MHz)

PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{REF}	V_{CC} – 1.5	V_{CC}	V_{CC}	V
	V_{AGND}	V_{SS}	V_{SS}	V_{SS}	V
Analog Input voltage	V_{AIN}	ADGND		A_{REF}	V
Supply Current for ADREF	I_{REF}	–	0.6	1.0	mA
Total error (Ta = 25 °C, VCC = V_{REF} = 5.0 V)		–	–	± 3	LSB

Characteristics of CTL AMP (Topr = − 20 to + 70 °C, V_{CC} = 5.0 V)

BLOCK	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	CONDITION
CTL BIAS AMP	No load output voltage	V_{CB}	2.4	2.5	2.6	V	No load
	Output voltage (with high load)	V_{CBH}	−	−	+ 70	mV	I si = 5 mA, Difference from V_{CB}
	Output voltage (with low load)	V_{CBL}	− 70	−	−	mV	I so = 5 mA, Difference from V_{CB}
REC CTL AMP	HIGH output voltage	V_{ROH}	3.2	−	−	V	I so = 5 mA
	LOW output voltage	V_{ROL}	−	−	1.8	V	I si = 5 mA
	D/A CONVERTER Differential error	V_{RDA}	−	−	$\pm\frac{1}{2}$	LSB	
	SW REC internal resistance	R_{REC}	55	85	130	Ω	Set to on by SWREC
PB CTL AMP	Input offset voltage	V_{COF}	− 15	−	+ 15	mV	RPCTL terminal
	Input bias current	I_{CIB1}	− 750	−	+ 750	nA	RPCTL terminal
		I_{CIB2}	− 750	−	+ 750	nA	CNFB terminal
	HIGH output voltage	V_{COH}	3.6	−	−	V	I so = 2 mA
	LOW output voltage	V_{COL}	−	−	1.2	V	I si = 2 mA
	Voltage gain	G_{C1}	−	60	−	dB	f : 1 kHz, Vin : 1mV, 60dB
		G_{C2}	−	51	−	dB	f : 10 kHz, Vin : 1mV, 60dB
	Feed back resistance	R_{SHORT}	5	10	20	kΩ	Fig3.20.1 (a) r3, SW internal resistance
		R_{AMP2}	20	40	60	kΩ	Fig3.20.1 (a) r4, SW internal resistance
	Resistance of Analog SW	R_{PB}	−	−	500	Ω	Set to on by SWPLY
		R_{BIAS}	−	−	500	Ω	Set to on by SWBAS
		R_{AMP0}	−	−	500	Ω	Set to on by <CAMP0>
		R_{AMP1}	−	−	500	Ω	Set to on by <CAMP1>
CTL PLUS SCHUMITTE	PDP Charge current	I_{CP}	4	−	−	mA	V_{COH} = 3.5V, V_{PDP} = 2.5V
	PDP Leakage current	I_{LP}	−	−	− 350	nA	V_{COL} = 1.5V, V_{PDP} = 2.5V R_{PDP} : OFF
	PDP Maximum output voltage	V_{OP}	4.3	4.7	−	V	Charge current : 0.1 mA
	PHSPDUP Resistance	R_{PDP}	5	10	20	kΩ	Fig3.20.1 (a) r5, r6, SW internal resistance
	1/2 level of Peak-hold Schmitt	V_{CSPA}	−	50	−	%	
	Manual Schmitt level	V_{CSP1}	−	100	−	mV	100 mV mode (to V_{CB})
		V_{CSP2}	−	200	−	mV	200 mV mode (to V_{CB})
		V_{CSP3}	−	300	−	mV	300 mV mode (to V_{CB})
		V_{CSP4}	−	500	−	mV	500 mV mode (to V_{CB})
	Noise Limit (plus)	V_{CSPL}	−	100	−	mV	(to V_{CB})
CTL MINUS SCHUMITTE	PDM Charge current	I_{CM}	− 4	−	−	mA	V_{COL} = 1.5V, V_{PDP} = 2.5V
	PDM Leakage current	I_{LM}	−	−	350	nA	V_{COL} = 3.5V, V_{PDP} = 2.5V R_{PDM} : OFF
	PDM Minimum output voltage	V_{OM}	−	0.3	0.7	V	Charge current : − 0.1 mA
	PHSPDUP Resistance	R_{PDM}	5	10	20	kΩ	
	1/2 level of Peak-hold Schmitt	V_{CSMA}	−	50	−	%	
	Manual Schmitt level	V_{CSM1}	−	− 100	−	mV	− 100 mV mode (to V_{CB})
		V_{CSM2}	−	− 200	−	mV	− 200 mV mode (to V_{CB})
		V_{CSM3}	−	− 300	−	mV	− 300 mV mode (to V_{CB})
		V_{CSM4}	−	− 500	−	mV	− 500 mV mode (to V_{CB})
	Noise Limit (minus)	V_{CSML}	−	− 100	−	mV	(to V_{CB})

Characteristics of CFG AMP (Topr = – 20 to + 70 °C, V_{CC} = 5.0 V)

BLOCK	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	CONDITION
CFG BIAS AMP	No load output voltage	V_{FB}	2.4	2.5	2.6	V	No load
	Output voltage (with high load)	V_{FBH}	–	–	+ 150	mV	I si = 5 mA, Difference from V_{FB}
	Output voltage (with low load)	V_{FBL}	– 150	–	–	mV	I so = 5 mA, Difference from V_{FB}
CFGA AMP	Input offset voltage	V_{FAOF}	– 15	–	+ 15	mV	
	Input bias voltage	V_{FAI}	– 750	–	+ 750	nA	
	HIGH output voltage	V_{FAOH}	4.3	4.7	–	V	I so = – 0.2 mA
	LOW output voltage	V_{FAOL}	–	0.3	0.7	V	I si = 0.2 mA
	Voltage gain	G_{FA1}	–	40	–	dB	f : 1 kHz, Vin : 10mV, 40dB
		G_{FA2}	–	37	–	dB	f : 10 kHz, Vin : 10mV, 40dB
CFGB AMP	Input offset voltage	V_{FBOF}	– 15	–	+ 15	mV	
	Input bias voltage	I_{FB1}	– 750	–	+ 750	nA	
	HIGH output voltage	V_{FBOH}	4.3	4.7	–	V	I so = – 0.2 mA
	LOW output voltage	V_{FBOL}	–	0.3	0.7	V	I si = 0.2 mA
	Voltage gain	G_{FB1}	–	40	–	dB	f : 1 kHz, Vin : 10mV, 40dB
		G_{FB2}	–	37	–	dB	f : 10 kHz, Vin : 1mV, 40dB
CFGA SCHMITT	P Schmitt Voltage 1	V_{FASP1}	–	80	–	mV	80 mV mode (to V_{FB})
	P Schmitt Voltage 2	V_{FASP2}	–	120	–	mV	120 mV mode (to V_{FB})
	M Schmitt Voltage 1	V_{FASM1}	–	– 80	–	mV	– 80 mV mode (to V_{FB})
	M Schmitt Voltage 2	V_{FASM2}	–	– 120	–	mV	– 120 mV mode (to V_{FB})
CFGB SCHMITT	P Schmitt Voltage 1	V_{FBSP1}	–	80	–	mV	80 mV mode (to V_{FB})
	P Schmitt Voltage 2	V_{FBSP2}	–	120	–	mV	120 mV mode (to V_{FB})
	M Schmitt Voltage 1	V_{FBSM1}	–	– 80	–	mV	– 80 mV mode (to V_{FB})
	M Schmitt Voltage 2	V_{FBSM2}	–	– 120	–	mV	– 120 mV mode (to V_{FB})

Characteristics of OSD AMP (Topr = – 20 to + 70 °C, V_{CC} = 5.0 V)

OUTPUT PIN	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
SC	Bias voltage	V_B	–	2.5	–	V	
	Burst amplitude	V_b	–	0.29	–	V (PP)	
	Chroma amplitude 1 / Burst amplitude	V_1 / V_b	–	2.0	–	–	
SY	Sync. tip level	V_S	–	1.60	–	V	
	Sync. to Pedestal	$\triangle V_{SP}$	–	0.60	–	V	$\triangle V_{SP} = V_P - V_S$
	Sync. to Luminance voltage 0	$\triangle V_{S0}$	–	0.66	–	V	$\triangle V_{S0} = V_0 - V_S$
	Sync. to Luminance voltage 1	$\triangle V_{S1}$	–	0.80	–	V	$\triangle V_{S1} = V_1 - V_S$
	Sync. to Luminance voltage 2	$\triangle V_{S2}$	–	1.08	–	V	$\triangle V_{S2} = V_2 - V_S$
	Sync. to Luminance voltage 3	$\triangle V_{S3}$	–	1.50	–	V	$\triangle V_{S3} = V_3 - V_S$
	Sync. to 100% White Level	$\triangle V_{SW}$	–	2.00	–	V	$\triangle V_{SW} = V_W - V_S$
OSD VIDEO	Color Burst amplitude	V_{Cb}	–	0.29	–	V_{P-P}	
	Chroma amplitude / Burst amplitude	V_C / V_{Cb}	–	2.0	–	–	
	Sync. tip level	VI_S	–	1.00	–	V	
	Sync. to Pedestal	$\triangle VI_{SP}$	–	0.30	–	V	$\triangle VI_{SP} = VI_P - VI_S$
	Sync. to Luminance voltage 0	$\triangle VI_{S0}$	–	0.33	–	V	$\triangle VI_{S0} = VI_0 - VI_S$
	Sync. to Luminance voltage 1	$\triangle VI_{S1}$	–	0.40	–	V	$\triangle VI_{S1} = VI_1 - VI_S$
	Sync. to Luminance voltage 2	$\triangle VI_{S2}$	–	0.54	–	V	$\triangle VI_{S2} = VI_2 - VI_S$
	Sync. to Luminance voltage 3	$\triangle VI_{S3}$	–	0.75	–	V	$\triangle VI_{S3} = VI_3 - VI_S$
	Sync. to 100% White Level	$\triangle VI_{SW}$	–	1.00	–	V	$\triangle VI_{SW} = VI_W - VI_S$

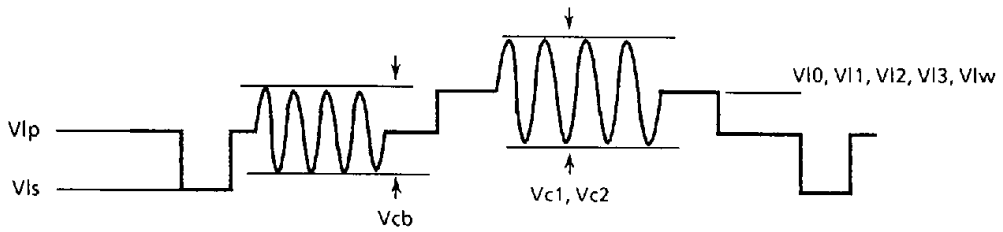


Fig. 4.1 OSD VIDEO Output Waveform

Characteristics of PV/BLK (Topr = − 20 to + 70 °C, V_{CC} = 5.00 V)

MODE	PARAMETER	SYMBOL	Min.	Typ.	Max.	UNIT	CONDITION
MIXOFF = 0	HIGH output voltage	V_H	4.70	5.00	5.00	V	I = + 100 μA
	MIDDLE-HIGH output voltage	VM2	3.00	3.30	3.60	V	I = ± 10 μA
	MIDDLE-LOW output voltage a	VM1a	1.30	1.60	2.0	V	I = ± 100 μA
	MIDDLE-LOW output voltage b	VM1b	1.30	1.60	2.0	V	I = ± 10 μA
	LOW output voltage	V_L	−	−	0.30	V	I = − 100 μA
MIXOFF = 1	HIGH output voltage	V_H	4.70	−	−	V	I = + 100 μA
	LOW output voltage	V_L	−	−	0.30	V	I = − 100 μA

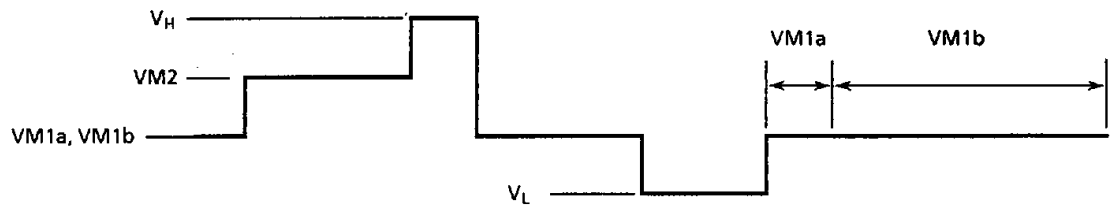


Fig. 4.2 PV / BLK Output Waveform

6. Peripheral Function Control Registers

6.1 Peripheral Function Control Registers

6.1.1 I/O area 1 (Direct Addressing Area)

Address	Symbol	Address	Symbol	Address	Symbol	Address	Symbol	Address	Symbol
FFB0	SYSCR1	FFC0	P0	FFD0	OSDDBR	FFE0	SC1BR	FFF0	TPG1DR
FFB1	SYSCR2	FFC1	P0CR	FFD1	TCCR2	FFE1	SC1CR	FFF1	SACR1
FFB2	TBCDR1	FFC2	P1	FFD2	TREG3	FFE2	SBICR1	FFF2	SACR2
FFB3	TBCDR2	FFC3	P1CR	FFD3	TCCR3	FFE3	SBIDBR	FFF3	SACR3
FFB4	P8	FFC4	P2	FFD4	TRUN	FFE4	I2CAR	FFF4	VIVACR1
FFB5		FFC5	P3	FFD5	PWM0L	FFE5	SBICR2	FFF5	VIVACR2
FFB6	CAPFST	FFC6	P4	FFD6	PWM0H	FFE6	I2CFCR1	FFF6	CAPICR2
FFB7	CAP0L	FFC7	P5	FFD7	PWM1L	FFE7	I2CFCR2	FFF7	CAPICR3
FFB8	CAP0M	FFC8	P6	FFD8	PWM1H	FFE8	I2CFDBR	FFF8	VASSDR
FFB9	CAP0H	FFC9	P7	FFD9	PWM2DR	FFE9	I2CFSR2	FFF9	CAPICR4
FFBA	CAP1L	FFCA	TREG0	FFDA	TPCR	FFEA	TPG0CR	FFFA	CAPICR5
FFBB	CAP1H	FFCB	TREG1	FFDB	TPDR	FFEB	TPG0L	FFFB	WDTCR1
FFBC	CAP2L	FFCC	TCCR1	FFDC	ADCR	FFEC	TPG0H	FFFC	WDTCR3
FFBD	CAP2H	FFCD	TREG2	FFDD	ADREG	FFED	TPG0DR	FFFD	CSYNCR
FFBE	CAPCR	FFCE	OSDCR	FFDE	SC0BR	FFEE	TPG1L		
FFBF	CAPICR1	FFCF	OSDADR	FFDF	SC0CR	FFEF	TPG1H		

6.1.2 I/O area 2

Address	Symbol	Address	Symbol
F780	P2CR	F790	IRF1
F781	P2MR	F791	IRF2
F782	P3CR	F792	ACCR
F783	P3MR	F793	PWMCR
F784	P4CR	F794	HACR
F785	P4MR	F795	RMTCR
F786	P5CR	F796	SACR4
F787	P5MR	F797	WDTCR2
F788	P7CR	F798	TBCCR
F789	ODMCR1	F799	PVCR
F78A	ODMCR2		
F78B	PW3L		
F78C	PW3H		
F78D	INTE1		
F78E	INTE2		
F78F	INTCR		

6.2 Peripheral Function Control Registers

6.2.1 System Clock Control Circuit

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
TBCCR	Time Base Counter Control Register	F798H			TBC1E	TBC0E	INTTBC11	INTTBC10	INTTBC01	INTTBC00
					R/W					
					0	0	0	0	0	0
					INTTBC Interrupt 00 :INTTBC Interrupt Disable 01 :INTTBC0 Interrupt Enable 10 :INTTBC1 Interrupt Enable 11 : INTTBC0/INTTBC1 Interrupt Enable		INTTBC1 Interrupt Source Clock Selection 00 :TBC12 01 :TBC14 10 :TBC16 11 :TBC18		INTTBC0 Interrupt Source Clock Selection 00 :TBC11 01 :TBC13 10 :TBC15 11 :TBC17	
TBCDR1	Time Base Counter Data Register 1	FFB2H	TBC12	TBC11	TBC10	TBC9	TBC8	TBC7	TBC6	TBC5
			R							
			0							
			Time Base Counter Data (TBC12 to 5)							
TBCDR2	Time Base Counter Data Register 2	FFB3H	TBC20	TBC19	TBC18	TBC17	TBC16	TBC15	TBC14	TBC13
			R							
			0							
			Time Base Counter Data (TBC20 to 13)							
SYSCR1	System Control Register1	FFB0H		SYSCK	XEN	XTEN	RXEN	RXTEN	RSYSCK	WUEF
				R/W						
				0	1	0	1	0	0	0
				System Clock Selection 0 : fc 1 : fs	High Frequency Oscillator Control 0 :Stop 1 :Restart Oscillation	Low Frequency Oscillator Control 0 :Stop 1 :Restart Oscillation	High Frequency Oscillator Control after restarting from stop mode 0 :Stop 1 :Restart Oscillation	Low Frequency Oscillator Control after restarting from stop mode 0 :Stop 1 :Restart Oscillation	Selection of System Clock Operation after restarting from Stop mode 0 : fc 1 : fs	Warming-up Counter Control 0 (W) : – 0 (R) : Warming-up Complete 1 (W) : Warming-up Start 1 (R) : In Warming-up
SYSCR2	System Control Register2	FFB1H				RTCCK	RTCST	RTCIS1	RTCIS0	WARM
						R/W				
						0	0	0	0	0
						RTC Source Clock Selection 0 : fs 1 : fc /4	RTC Start Control 0 : Stop & Clear 1 : Start	Interval Time Control of RTC Interrupt 00 : $fc/2^{15}$ or $fs/2^{15}$ [Hz] 01 : $fc/2^{16}$ or $fs/2^{16}$ [Hz] 10 : $fc/2^{14}$ or $fs/2^{14}$ [Hz] 11 :Don't use		Warming-up Time 0 : $2^{14}/fc$ or $2^{14}/fs$ [s] 1 : $2^{16}/fc$ or $2^{16}/fs$ [s]

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
WDTCR1	Watch-dog Timer Control Register1	FFFBH			TBC	TBC0F	WDTE		EXF	DRVE
					R/W	R/W	R/W		R	R/W
					0	0	1		0	0
					!NTTBC1 Interrupt Request Flag 0(W) : Clear 1(R) : Interrupt Request	!NTTBC0 Interrupt Request Flag 0(W) : Clear 1(R) : Interrupt Request	WDT Enable 0 : Disable 1 : Enable		Invert each time Exx instruction is executed	Controlling output status for port during Stop mode 0 : High Impedance 1 : Keep the status throughout setting Stop mode
WDTCR2	Watch-dog Timer Control Register2	F797H					WDTP1	WDTP0	HALTM1	HALTM0
							R/W		R/W	
							0	0	0	0
							WDT Source Clock Selection 00 : TBC20 01 : TBC18 10 : TBC16 11 : TBC10		Standby mode Selection 00 : – 01 : STOP mode 10 : IDLE/SLEEP mode 11 : Don't use	

6.2.2 Interrupt Control Circuit

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
IRF1	Interrupt Request Flag 1	F790H	IRFT0DIR	IRFTBC	IRFIIC	IRFTPG1	IRFTPG0	IRFCAP0	IRFCAP1	IRF0
			R/W (Only clear code can be written into IRF1)							
			0	0	0	0	0	0	0	0
			Interrupt Request Flag 0 : No Interrupt Request 1 : Interrupt Request							
IRF2	Interrupt Request Flag 2	F791H	IRFRTC	IRF1	IRFVA	IRFT3AD	IRFT2	IRFT1	IRFSIO1	IRFSIO0
			R							
			0	0	0	0	0	0	0	0
			Interrupt Request Flag 0 : No Interrupt Request 1 : Interrupt Request							
INTE1	Interrupt Enable Register 1	F78DH	IET0DIR	IETBC	IEIIC	IETPG1	IETPG0	IECAP0	IECAP1	IE0
			R/W							
			0	0	0	0	0	0	0	0
			INTT0DIR Interrupt 0 : Disable 1 : Enable	INTTBC Interrupt 0 : Disable 1 : Enable	INTIIC Interrupt 0 : Disable 1 : Enable	INTTPG1 Interrupt 0 : Disable 1 : Enable	INTTPG0 Interrupt 0 : Disable 1 : Enable	INTCAP0 Interrupt 0 : Disable 1 : Enable	INTCAP1 Interrupt 0 : Disable 1 : Enable	INT0 Interrupt 0 : Disable 1 : Enable
INTE2	Interrupt Enable Register 2	F78EH	IERTC	IE1	IEVA	IET3AD	IET2	IET1	IESIO1	IESIO0
			R/W							
			0	0	0	0	0	0	0	0
			INTRTC Interrupt 0 : Disable 1 : Enable	INT1 Interrupt 0 : Disable 1 : Enable	INTVA Interrupt 0 : Disable 1 : Enable	INTT3AD Interrupt 0 : Disable 1 : Enable	INTT2 Interrupt 0 : Disable 1 : Enable	INTT1 Interrupt 0 : Disable 1 : Enable	INTSIO1 Interrupt 0 : Disable 1 : Enable	INTSIO0 Interrupt 0 : Disable 1 : Enable
INTCR	Interrupt Control Register	F78FH			CLKCK	$\overline{CLOE}$	INTTPG0E	INTTPG0S	T3ADS	T0DIRS
					R/W		R/W		R/W	
					0	0	0	0	0	0
					CLK Output Frequency selection 0 : fc/4 or fs/4 1 : fc/2 or fs/2	CLK Output 0 : Disable 1 : Enable	INTTPG0 (TPG03) Edge Selection 0 : TPG03 ↑ 1 : TPG03 ↓	INTTPG0 (TPG03) Interrupt 0 : Disable 1 : Enable	INTT3AD Interrupt Source Selection 0 : INTT3 1 : INTAD	INTT0DIR Interrupt Source Selection 0 : INTT0 1 : INTDIR

6.2.3 Watch-dog Timer (WDT)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
WDTCR1	Watch-dog Timer Control Register 1	FFFBH			TBC1F	TBC0F	WDTE		EXF	DRVE
					R/W	R/W	R/W		R	R/W
					0	0	0		0	0
					INTTBC1 Interrupt Request Flag 0 (W) : Clear 1 (R) : Interrupt Request	INTTBC0 Interrupt Request Flag 0 (W) : Clear 1 (R) : Interrupt Request	WDT Enable 0 : Disable 1 : Enable		Invert each time EXX instruction is executed	Output control in STOP mode 0 : High Impedance 1 : Keep the status throughout setting STOP mode
WDTCR2	Watch-dog Timer Control Register 2	F797H					WDTP1	WDTP0	HALTM1	HALTM0
							R/W		R/W	
							0	0	0	0
							WDT Source Clock Selection 00 : TBC20 01 : TBC18 10 : TBC16 11 : TBC10		Standby mode Selection 00 : – 01 : STOP mode 10 : IDLE/SLEEP mode 11 : Don't use	
WDTCR3	Watch-dog Timer Control Register 3	FFFCH	Watch-dog Timer Control Code Register							
			W							
			B1H : WDT Disable 4EH : WDT Clear Others : –							

6.2.4 Timer Counter

(1) Timer Counter 0 (TC0) / Timer Counter 1 (TC1)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
TREG0	Timer Counter0 Data Register	FFCAH	TC/TR07	TC/TR06	TC/TR05	TC/TR04	TC/TR03	TC/TR02	TC/TR01	TC/TR00
			R/W							
			0 / *	0 / *	0 / *	0 / *	0 / *	0 / *	0 / *	0 / *
TREG1	Timer Counter1 Data Register	FFCBH	TC/TR17	TC/TR16	TC/TR15	TC/TR14	TC/TR13	TC/TR12	TC/TR11	TC/TR10
			R/W							
			0 / *	0 / *	0 / *	0 / *	0 / *	0 / *	0 / *	0 / *
TCCR1	Timer Counter Control Register 1	FFCCH	CLBC16	CLBC1	CLBC0	TMOD	T1CLK1	T1CLK0	T0CLK1	T0CLK0
			R/W							
			0	0	0	0	0	0	0	0
			16 bit counter clear 0 : Disable 1 : Enable	TC1 counter clear 0 : Disable 1 : Enable	TC0 counter clear 0 : Disable 1 : Enable	Timer mode selection 0 : 8 bit 1 : 16 bit	TC1 source clock selection 00 : TO0TRG (TC0 comparator output) 01 : TBC6 10 : TBC10 11 : TBC14		TC0 source clock selection 00 : TI0 (Input from P34) 01 : CFGTM (Input from CAPIN) 10 : TBC6 11 : TBC10	
TCCR2	Timer Counter Control Register 2	FFD1H			T1CL	T0CL	CLBC2	T2CL	T2CLK1	T2CLK0
					R/W		R/W			
					0	0	0	0	0	0
					TC1 counter forced clear 0 : – 1 : Clear	TC0 counter forced clear 0 : – 1 : Clear	TC2 counter Clear 0 : Disable 1 : Enable	TC2 counter forced clear 0 : – 1 : Clear	TC2 source clock selection 00 : PCTLA (Input from CAPIN) 01 : TI2 (Input from P35) 10 : TBC6 11 : TBC10	
TRUN	Timer Start Control Register	FFD4H	PWM3RUN	T3RUN	PWM1RUN	PWM0RUN	PWM2RUN	T2RUN	T1RUN	T0RUN
			R/W	R/W	R/W		R/W	R/W	R/W	
			0	0	0	0	0	0	0	0
			PWM3 0 : Stop 1 : Start	TC3 0 : Stop 1 : Start	PWM1 0 : Stop 1 : Start	PWM0 0 : Stop 1 : Start	PWM2 0 : Stop 1 : Start	TC2 0 : Stop 1 : Start	TC1 0 : Stop 1 : Start	TC0 0 : Stop 1 : Start

(2) Timer Counter2 (TC2)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
TREG2	Timer Counter2 Data Register	FFCDH	TC/TR27	TC/TR26	TC/TR25	TC/TR24	TC/TR23	TC/TR22	TC/TR21	TC/TR20
			R/W							
			0 / *	0 / *	0 / *	0 / *	0 / *	0 / *	0 / *	0 / *
TCCR2	Timer Counter Control Register 2	FFD1H			T1CL	T0CL	CLBC2	T2CL	T2CLK1	T2CLK0
					R/W		R/W			
					0	0	0	0	0	0
					TC1 counter forced clear 0 : – 1 : Clear	TC0 counter forced clear 0 : – 1 : Clear	TC2 counter Clear 0 : Disable 1 : Enable	TC2 counter forced clear 0 : – 1 : Clear	TC2 source clock selection 00 : PCTLA (Input from CAPIN) 01 : TI2 (Input from P35) 10 : TBC6 11 : TBC10	
TRUN	Timer Start Control Register	FFD4H	PWM3RUN	T3RUN	PWM1RUN	PWM0RUN	PWM2RUN	T2RUN	T1RUN	T0RUN
			R/W	R/W	R/W		R/W	R/W	R/W	
			0	0	0	0	0	0	0	0
			PWM3 0 : Stop 1 : Start	TC3 0 : Stop 1 : Start	PWM1 0 : Stop 1 : Start	PWM0 0 : Stop 1 : Start	PWM2 0 : Stop 1 : Start	TC2 0 : Stop 1 : Start	TC1 0 : Stop 1 : Start	TC0 0 : Stop 1 : Start

(3) Timer Counter 3 (TC3)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
TREG3	Timer Counter 3 Data Register	FFD2H	TC/TR37	TC/TR36	TC/TR35	TR34	TC/TR33	TC/TR32	TC/TR31	TC/TR30
			R/W							
			0/*	0/*	0/*	0/*	0/*	0/*	0/*	0/*
TCCR3	Timer Counter Control Register 3	FFD3H	TR3DE	TFF3C1	TFF3C0	TFF3IE	T3MOD	T3CL	T3CLK1	T3CLK0
			R/W	W		R/W	R/W	R/W	R/W	
			0	*	*	0	0	0	0	0
			TREG3 Shift-Trigger Selection 0 : Writing data on TREG3 1 : Over flow	Timer 3 Flip-flop (TFF) Control 00 : Forced invert 01 : Forced set 10 : Forced reset 11 : Keep TO3 output		TFF Output Inverted 0 : Disable 1 : Enable	TC3 mode Selection 0 : PWM mode 1 : Timer mode	TC3 Counter Clear 0 : – 1 : Clear	TC3 Source Clock Selection 00 : TBC2 01 : TBC6 10 : TBC11 11 : TI3 (Input from P24)	
TRUN	Timer Start Control Register	FFD4H	PWM3RUN	T3RUN	PWM1RUN	PWM0RUN	PWM2RUN	T2RUN	T1RUN	T0RUN
			R/W	R/W	R/W		R/W	R/W	R/W	
			0	0	0	0	0	0	0	0
			PWM3 0 : Stop 1 : Start	TC3 0 : Stop 1 : Start	PWM1 0 : Stop 1 : Start	PWM0 0 : Stop 1 : Start	PWM2 0 : Stop 1 : Start	TC2 0 : Stop 1 : Start	TC1 0 : Stop 1 : Start	TC0 0 : Stop 1 : Start

6.2.5 Capture

(1) Capture Input Control Circuit (CAPIN)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
CAPICR1	Capture Input Control Register 1	FFBFH	CAP2E	CAP1E	CAP05E	CAP04E	CAP03E	CAP02E	CAP01E	CAP00E
			R/W							
			0	0	0	0	0	0	0	0
			CAP0 / CAP1 / CAP2 Trigger Input Disable / Enable 0 : Disable 1 : Enable							
CAPICR2	Capture Input Control Register 2	FFF6H	PCTLCK2	PCTLCK1	PCPR5	PCPR4	PCPR3	PCPR2	PCPR1	PCPR0
			R/W		R/W					
			0	0	0	0	0	0	0	0
			CTL Duty Discriminating Circuit Source Clock Selection 00 : TBC3 10 : TBC7 01 : TBC5 11 : TBC10		6-bit Programmable Clock Divider Control Divider Setting 1/1 to 1/64 from CTLIN (from 30), CTLOUT from (CTLAmp) CFGA (from CFG Amp)					
CAPICR3	Capture Input Control Register 3	FFF7H						DPCP2	DPCP1	DPCP0
								R/W		
								0	0	0
								3-bit programmable clock divider Divider Setting 1/1 to 1/8 from DPGPF from P31		
CAPICR4	Capture Input Control Register 4	FFF9H			EXTVS	EXTEG	DFGPGEG	CFGWPR	CFGAEG	CTLEG
					R/W					
					0	0	0	0	0	0
					EXT/VS (to CAP0) Input Selection 0 : VSYNC (from CSYNC) 1 : EXT (from P34)	EXT (P34) Trigger Edge Selector 0 : ↑ 1 : ↓	DFGPG Input (from P31) Edge Selection 0 : ↑ 1 : ↓	Dividing rate selection for CFGA input 0 : 1/1 1 : 1/2	CFGA Input Edge Selection 0 : ↑ ↓ 1 : ↑	CTLIN / CTLOUT Input Edge Selection 0 : ↑ 1 : ↑ ↓
CAPICR5	Capture Input Control Register 5	FFFAH			CTLSEL	RMTST	RMTPO	ACCKBP	RMTBP	CFGMCP
					R/W	R/W	R/W	R/W	R/W	R
					0	0	0	0	0	0
					CTL Input (to CAP0) Selection 0 : CTLOUT (from CTL Amp) 1 : CTLIN (from P30)	Remote-Control Signal Input Control 0 : STOP 1 : Start	Remote-Control Signal Input Polarity Selection 0 : Positive 1 : Negative	AC Clock Input Control 0 : Sampling 1 : Bypass	Remote-Control Signal Input Bypass 0 : Omission Compensation/Noise Removal 1 : Bypass	CFG Flag 0 : Normal operation 1 : Error detection
CAPCR	Capture Control Register	FFBEH	CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS
			R	R	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			CAP2 Trigger Input 0 : No Trigger Input 1 : Trigger Input	CAP1 Trigger Input 0 : No Trigger Input 1 : Trigger Input	CAP1/CAP2 Status Clear 0 : – 1 : Clear	VISS Detection Flag 0 : – 1 : Clear	VASS Detect ion Flag 0 : – 1 : Clear	TPG0 FIFO Address 0 : – 1 : Clear	CFG Flag Clear 0 : – 1 : Clear	CAP0 FIFO Counter / Status 0 : – 1 : Clear

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
VIVACR2	VISS/ VASS Control Register 2	FFF5H	PCTLPO	PCTLCKS	$\overline{CDIV}$	$\overline{MSK}$	VISS3	VISS2	VISS1	VISS0
			R/W	R/W	R/W	R/W	R/W			
			0	0	0	0	0	0	0	0
			CTL Signal Duty Discriminating Polarity Switch 0 : Positive 1 : Negative	CTL Duty Discriminating Circuit Source Clock Selection 0 : Manual Switch 1 : Automatic Switch	CTLIN/CTLOUT Input Divider Control 0 : Divider 1 : Bypass	CFGA Input Mask Control 0 : Mask 1 : Bypass	Setting Comparator data of VISS detect Circuit Setting 4-bit data of 0H to FH			

(2) Capture0 (CAP0)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
CAPFST	Capture0 FIFO Status Register	FFB6H	CAPF7	CAPF6	CAPF5	CAPF4	CAPF3	CAPF2	CAPF1	CAPF0
			R							
			0	0	0	0	0	0	0	0
			Capture0 (CAP0) FIFO status 0 : No-capture data 1 : Capture data							
CAP0L	Capture0 Lower Data Register	FF87H	CAP0D7	CAP0D6	CAP0D5	CAP0D4	CAP0D3	CAP0D2	CAP0D1	CAP0D0
			R							
			*	*	*	*	*	*	*	*
			Capture0 (CAP0) lower data register							
CAP0M	Capture0 Middler Data Register	FFB8H	CAP0D15	CAP0D14	CAP0D13	CAP0D12	CAP0D11	CAP0D10	CAP0D9	CAP0D8
			R							
			–							
			Capture0 (CAP0) middle data register							
CAP0H	Capture0 Higher Data Register	FFB9H	CAP0T5 (EXTVS)	CAP0T4 (ACCK)	CAP0T3 (CTL)	CAP0T2 (VS)	CAP0T1 (RMTD)	CAP0T0 (RMTU)	CAP0D17	CAP0D16
			R						R	
			*	*	*	*	*	*	*	*
			Capture0 (CAP0) trigger input status 0 : No-trigger input 1 : trigger input						Capture0 (CAP0) higher data register	
CAPCR	Capture Control Register	FFBEH	CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS
			R	R	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			CAP2 trigger input status 0 : No trigger input 1 : Trigger input	CAP1 trigger input status 0 : No trigger input 1 : Trigger input	CAP1/CAP2 status clear 0 : – 1 : Clear	VISS detect flag 0 : – 1 : Clear	VASS detect flag 0 : – 1 : Clear	TPG0 FIFO address 0 : – 1 : Clear	Clear of CFG flag 0 : – 1 : Clear	CAP0 FIFO counter / status 0 : – 1 : Clear

(3) Capture1 (CAP1)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
CAP1L	Capture1 Lower Data Register	FFBAH	CAP1D7	CAP1D6	CAP1D5	CAP1D4	CAP1D3	CAP1D2	CAP1D1	CAP1D0
			R							
			*	*	*	*	*	*	*	*
			Capture1 lower data register							
CAP1H	Capture1 Higher Data Register	FFBBH	CAP1D15	CAP1D14	CAP1D13	CAP1D12	CAP1D11	CAP1D10	CAP1D9	CAP1D8
			R							
			*	*	*	*	*	*	*	*
			Capture1 higher data register							
CAPCR	Capture Control Register	FFBEH	CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS
			R	R	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			CAP2 trigger input status 0 : No trigger input 1 : Trigger input	CAP1 trigger input status 0 : No trigger input 1 : Trigger input	CAP1/CAP2 status clear 0 : – 1 : Clear	VISS detect flag 0 : – 1 : Clear	VASS detect flag 0 : – 1 : Clear	TPG0 FIFO address 0 : – 1 : Clear	Clear of CFG flag 0 : – 1 : Clear	CAP0 FIFO counter / status 0 : – 1 : Clear

(4) Capture2 (CAP2)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
CAP2L	Capture2 Lower Data Register	FFBCH	CAP2D7	CAP2D6	CAP2D5	CAP2D4	CAP2D3	CAP2D2	CAP2D1	CAP2D0
			R							
			*	*	*	*	*	*	*	*
			Capture2 lower data register							
CAP2H	Capture2 Higher Data Register	FFBDH	CAP2D15	CAP2D14	CAP2D13	CAP2D12	CAP2D11	CAP2D10	CAP2D9	CAP2D8
			R							
			*	*	*	*	*	*	*	*
			Capture2 higher data register							
CAPCR	Capture Control Register	FFBEH	CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS
			R	R	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			CAP2 trigger input status 0 : No trigger input 1 : Trigger input	CAP1 trigger input status 0 : No trigger input 1 : Trigger input	CAP1/CAP2 status clear 0 : – 1 : Clear	VISS detect flag 0 : – 1 : Clear	VASS detect flag 0 : – 1 : Clear	TPG0 FIFO address 0 : – 1 : Clear	Clear of CFG flag 0 : – 1 : Clear	CAP0 FIFO counter / status 0 : – 1 : Clear

6.2.6 AC Clock Input Cirucuit (ACCK)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
ACCR	AC Noise Removal Control Register	F792H						ACCKST	ACKS1	ACKS0
								R/W	R/W	
								0	0	0
								AC Clock Sampling 0 : Stop 1 : Start	AC Clock Sampling rate Selection 00 : TBC10 01 : TBC11 10 : TBC12 11 : TBC13	
CAPCR5	Capture Input Control Register5	FFFAH			CTLSEL	RMTST	RMTPO	ACCKBP	RMTBP	CFGMCP
					R/W	R/W	R/W	R/W	R/W	R
					0	0	0	0	0	0
					CTL input (to CAP0) Selection 0 : CTLOUT (from CTL Amp) 1 : CTLIN (from P30)	Remote-Control Signal Control 0 : Stop 1 : Start	Remote-Control signal Input Polarity Selection 0 : Positive 1 : Negative	AC Clock Input Control 0 : Sampling 1 : By-pass	Remote-Control Signal Input Bypass 0 : Omission Compensation / Noise Removal 1 : Bypass	CFG flag 0 : Normal Operation 1 : Error detection

6.2.7 Remote Control Signal Input Circuit (RMTIN)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
RMTCR	RMTIN Control Register	F795H	RMTD7	RMTD6	RMTD5	RMTD4	RMTD3	RMTD2	RMTD1	RMTD0
			R/W				R/W			
			0	0	0	0	0	0	0	0
			Noise cancel width Comparative value of 4-bit counter (Noise canceller)				Missing correction width Comparative value of 4-bit counter (Loss recovery)			
CAPCR5 CAPICR5	Capture Input Control Register5	FFFAH			CTLSEL	RMTST	RMTPO	ACCKBP	RMTBP	CFGMCP
					R/W	R/W	R/W	R/W	R/W	R
					0	0	0	0	0	0
					CTL input (to CAP0) Selection 0 : CTLOUT (from CTL Amp) 1 : CTLIN (from P30)	Remote-Control Signal Control 0 : Stop 1 : Start	Remote-Control signal Input Polarity Selection 0 : Positive 1 : Negative	AC Clock Input Control 0 : Sampling 1 : By-pass	Remote-Control Signal Input Bypass 0 : Omission Compensation / Noise Removal 1 : Bypass	CFG flag 0 : Normal Operation 1 : Error detection

6.2.8 Timing Pulse Generator

(1) Timing Pulse Generator 0 (TPG0)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
TPG0CR	TPG 0 Control Register	FFEAH				FEMPIE	TPFUL0	TPEMP0	TPF01	TPF00
						W	R	R	R	
						0	0	1	0	0
						INTTPG0 (Empty) Interrupt 0 : – 1 : Enable	TPG0 FIFO Full flag 0 : – 1 : Full	TPG0 FIFO Empty flag 0 : – 1 : Empty	TPG0 FIFO Status flag 00 : Empty or full 01 : 1 Data 10 : 2 Data 11 : 3 Data	
TPG0L	TPG 0 Lower Timing Data Register	FFEBH	TPG0D7	TPG0D6	TPG0D5	TPG0D4	TPG0D3	TPG0D2	TPG0D1	TPG0D0
			W							
			*	*	*	*	*	*	*	*
			TPG0 Timing Data							
TPG0H	TPG 0 Higher Timing Data Register	FFECH	TPG0D15	TPG0D14	TPG0D13	TPG0D12	TPG0D11	TPG0D10	TPG0D9	TPG0D8
			W							
			*	*	*	*	*	*	*	*
			TPG0 Timing Data							
TPG0DR	TPG 0 Output Data Register	FFEDH			TPGD05	TPGD04	TPGD03	TPGD02	TPGD01	TPGD00
					W					
					*	*	*	*	*	*
					TPG0 Output Data					
CAPCR	Capture Control Register	FFBEH	CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS
			R	R	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			CAP2 Input Trigger Status 0 : No Trigger Input 1 : Trigger Input	CAP2 Input Trigger Status 0 : No Trigger Input 1 : Trigger Input	CAP1/CAP2 Status Clear 0 : – 1 : Clear	VISS Detect Flag Clear 0 : – 1 : Clear	VASS Detect Flag Clear 0 : – 1 : Clear	TPG0 FIFO Address 0 : – 1 : Clear	CFG Flag Clear 0 : – 1 : Clear	CAP0/FIFO Counter / Status 0 : – 1 : Clear
INTCR	Interrupt Control Register	F78FH			CLKCK	CLOE	INTTPG0E	INTTPG0S	T3ADS	T0DIRS
					R/W		R/W		R/W	
					0	0	0	0	0	0
					CLK Output Frequency Selection 0 : fc/4 or fs/4 1 : fc/2 or fs/2	CLK Output 0 : Enable 1 : Disable	INTTPG0 (TPG03) Edge Selection 0 : TPG03 ↑ 1 : TPG03 ↓	INTTPG0S (TPG03) Interrupt 1 : Disable 1 : Enable	INTT3AD Interrupt Request Selection 0 : INTT3 1 : INTAD	INTT0DIR Interrupt Request Selection 0 : INTT0 1 : INTDIR

(2) Timing Pulse Generator1 (TPG1)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
TPG1L	TPG1 Lower Timing Data Register	FFEEH	TPG1D7	TPG1D6	TPG1D5	TPG1D4	TPG1D3	TPG1D2	TPG1D1	TPG1D0
			W							
			*	*	*	*	*	*	*	*
			TPG1 Lower Timing Data							
TPG1H	TPG1 Higher Timing Data Register	FFEFH	TPG1DF	TPG1DE	TPG1DD	TPG1DC	TPG1DB	TPG1DA	TPG1D9	TPG1D8
			W							
			*	*	*	*	*	*	*	*
			TPG1 Higher Timing Data							
TPG1DR	TPG1 Output data Register	FFF0H					TPGD13	TPGD12	TPGD11	TPGD10
							W			
							*	*	*	*
							TPG1 Output Data			

6.2.9 Pulse Width Modulation Output

(1) 12-bit PWM (PWM0, PWM1)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
PWM0L	PWM0 Lower Data Register	FFD5H	PWM0D7	PWM0D6	PWM0D5	PWM0D4	PWM0D3	PWM0D2	PWM0D1	PWM0D0
			W							
			*	*	*	*	*	*	*	*
PWM0H	PWM0 Higher Data Register	FFD6H					PWM0D11	PWM0D10	PWM0D9	PWM0D8
							W			
							*	*	*	*
PWM1L	PWM1 Lower Data Register	FFD7H	PWM1D7	PWM1D6	PWM1D5	PWM1D4	PWM1D3	PWM1D2	PWM1D1	PWM1D0
			W							
			*	*	*	*	*	*	*	*
PWM1H	PWM1 Higher Data Register	FFD8H					PWM1D11	PWM1D10	PWM1D9	PWM1D8
							W			
							*	*	*	*
TRUN	Timer Start Control Register	FFD4H	PWM3RUN	T3RUN	PWM1RUN	PWM0RUN	PWM2RUN	T2RUN	T1RUN	T0RUN
			R/W	R/W	R/W		R/W	R/W	R/W	
			0	0	0	0	0	0	0	0
			PWM3 0 : Stop 1 : Start	TC3 0 : Stop 1 : Start	PWM1 0 : Stop 1 : Start	PWM0 0 : Stop 1 : Start	PWM2 0 : Stop 1 : Start	TC2 0 : Stop 1 : Start	TC1 0 : Stop 1 : Start	TC0 0 : Stop 1 : Start
PWMCR	PWM Control Reigster	F793H		PWM01M	CFRTRGS	SYNCPO	PWMSEL	PWMPO2	PWMPO1	PWMPO0
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
				0	0	0	0	0	0	0
				PWM0/PWM1 Carrier Frequency Selection 0 : 20.83 kHz 1 : 41.67 kHz	CAPFR (P37) Trigger Edge Selection 0 : ↑ 1 : ↓	CSYNC Input Polarity Selection 0 : Positive 1 : Invert	PWM2/PWM3 (P74) Output Selection 0 : PWM2 1 : PWM3	PWM2/PWM3 Output Polarity Selection 0 : Positive 1 : Invert	PWM1 Output Polarity Selection 0 : Positive 1 : Invert	PWM0 Output Polarity Selection 0 : Positive 1 : Invert
ODMCR1	Open-drain Control Register 1	F789H	PWM1OC	PWM0OC	P37OC	P24OC	P23OC	P22OC	P21OC	P20OC
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			PWM1 Output Control 0 : Push-pull 1 : Open-drain	PWM0 Output Control 0 : Push-pull 1 : Open-drain	P37 Output Control 0 : Push-pull 1 : Open-drain	P24 Output Control 0 : Push-pull 1 : Open-drain	P23 Output Control 0 : Push-pull 1 : Open-drain	P22 Output Control 0 : Push-pull 1 : Open-drain	P21 Output Control 0 : Push-pull 1 : Open-drain	P20 Output Control 0 : Push-pull 1 : Open-drain

(2) 8-bit PWM (PWM2)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
PW2DR	PWM2 Data Register	FFD9H	PWM2D7	PWM2D6	PWM2D5	PWM2D4	PWM2D3	PWM2D2	PWM2D1	PWM2D0
			W							
			*	*	*	*	*	*	*	*
TRUN	Timer Start Control Register	FFD4H	PWM3RUN	T3RUN	PWM1RUN	PWM0RUN	PWM2RUN	T2RUN	T1RUN	T0RUN
			R/W	R/W	R/W		R/W	R/W	R/W	
			0	0	0	0	0	0	0	0
			PWM3 0 : Stop 1 : Start	TC3 0 : Stop 1 : Start	PWM1 0 : Stop 1 : Start	PWM0 0 : Stop 1 : Start	PWM2 0 : Stop 1 : Start	TC2 0 : Stop 1 : Start	TC1 0 : Stop 1 : Start	TC0 0 : Stop 1 : Start
PWMCR	PWM Control Register	F793H		PWM01M	CFRTRGS	SYNCPO	PWMSEL	PWMPO2	PWMPO1	PWMPO0
				R/W	R/W	R/W	R/W	R/W		R/W
				0	0	0	0	0	0	0
				PWM0/PWM1 Carrier Frequency Selection 0 : 20.83 kHz 1 : 41.67 kHz	CAPFR (P37) Trigger Edge Selection 0 : ↑ 1 : ↓	CSYNC Input Polarity Selection 0 : Positive 1 : Invert	PWM2/PWM3 (P74) Output Selection 0 : PWM2 1 : PWM3	PWM2/PWM3 Output Polarity Selection 0 : Positive 1 : Invert	PWM1 Output Polarity Selection 0 : Positive 1 : Invert	PWM0 Output Polarity Selection 0 : Positive 1 : Invert
ODMCR2	Open-drain Control Register 2	F78AH				P74OC	P56OC	P55OC	P53OC	P52OC
						R/W	R/W	R/W	R/W	R/W
						0	0	0	0	0
						P74 Output Control 0 : Push-pull 1 : Open-drain	P56 Output Control 0 : Push-pull 1 : Open-drain	P55 Output Control 0 : Push-pull 1 : Open-drain	P53 Output Control 0 : Push-pull 1 : Open-drain	P52 Output Control 0 : Push-pull 1 : Open-drain

(3) 14 bit PWM (PWM3)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
PWM3DRL	PWM3 Lower Data Register	F78BH	PWM3D7	PWM3D6	PWM3D5	PWM3D4	PWM3D3	PWM3D2	PWM3D1	PWM3D0
			W							
			*	*	*	*	*	*	*	*
PWM3DRH	PWM3 Higher Data Register	F78CH			PWM3D13	PWM3D12	PWM3D11	PWM3D10	PWM3D9	PWM3D8
			W							
					*	*	*	*	*	*
TRUN	Timer Start Control Register	FFD4H	PWM3RUN	T3RUN	PWM1RUN	PWM0RUN	PWM2RUN	T2RUN	T1RUN	T0RUN
			R/W	R/W	R/W		R/W	R/W	R/W	
			0	0	0	0	0	0	0	0
			PWM3 0 : Stop 1 : Start	TC3 0 : Stop 1 : Start	PWM1 0 : Stop 1 : Start	PWM0 0 : Stop 1 : Start	PWM2 0 : Stop 1 : Start	TC2 0 : Stop 1 : Start	TC0 0 : Stop 1 : Start	TC1 0 : Stop 1 : Start
PWMCR	PWM Control Register	F793H		PWM01M	CFRTRGS	SYNCPO	PWMSEL	PWMPO2	PWMPO1	PWMPO0
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
				0	0	0	0	0	0	0
				PWM0/PWM1 Carrier Frequency Selection 0 : 20.83 kHz 1 : 41.67 kHz	CAPFR (P37) Trigger Edge Selection 0 : ↑ 1 : ↓	CSYNC Input Polarity 0 : Push-Pull 1 : Open-drain	PWM2/PWM3 Output Selection 0 : PWM2 1 : PWM3	PWM2/PWM3 Output Polarity Selection 0 : Positive 1 : Invert	PWM1 Output Polarity Selection 0 : Positive 1 : Invert	PWM0 Output Polarity Selection 0 : Positive 1 : Invert
ODMCR2	Open-drain Control Register2	F78AH				P74OC	P56OC	P55OC	P53OC	P52OC
						R/W	R/W	R/W	R/W	R/W
						0	0	0	0	0
						P74 Output Control 0 : Push-Pull 1 : Open-drain	P56 Output Control 0 : Push-Pull 1 : Open-drain	P55 Output Control 0 : Push-Pull 1 : Open-drain	P53 Output Control 0 : Push-Pull 1 : Open-drain	P52 Output Control 0 : Push-Pull 1 : Open-drain

6.2.10 VISS / VASS Detection Circuit (VIVA)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
VIVACR1	VISS/ VASS Control Register 1	FFF4H	"0"	"0"	"0"	"0"		CTLDTY	VISSFL	VASSFL
			R/W	R/W	R/W	R/W		R		
			0	0	0	0		*	0	0
			Always Write "0"	Always Write "0"	Always Write "0"	Always Write "0"		CTL duty discriminating Output Monitor 0 : CTLduty ≥ 50 % 1 : CTLduty < 50 %	VISS Detection flag 0 : – 1 : VISS detect	VASS Detection flag 0 : – 1 : VASS detect
VIVACR2	VISS/ VASS Control Register 2	FFF5H	PCTLPO	PCTLCKS	$\overline{CDIV}$	$\overline{MSK}$	VISS3	VISS2	VISS1	VISS0
			R/W	R/W	R/W	R/W	R/W			
			0	0	0	0	0	0	0	0
			CTL Signal Duty discriminating Polarity Switch 0 : Positive 1 : Negative	CTL Duty discriminating Circuit Source Clock Selection 0 : Manual Switch 1 : Automatic Switch	CTLIN/CTLOUT Input Divider Control 0 : Divider 1 : Bypass	CFGA Input Mask Control 0 : Mask 1 : Bypass	Setting comparator data of VISS detection circuit Setting 4-bit data 0H to FH			
VASSDR	VASS Data Register	FFF8H	VASS7	VASS6	VASS5	VASS4	VASS3	VASS2	VASS1	VASS0
			R							
			*	*	*	*	*	*	*	*
			VASS Data Lower 8-bit							
			VASS15	VASS14	VASS13	VASS12	VASS11	VASS10	VASS9	VASS8
			R							
			*	*	*	*	*	*	*	*
			VASS Data Higher 8-bit							
CAPICR2	Capture Input Control Register 2	FFF6H	PCTLCK1	PCTLCK0	PCPR5	PCPR4	PCPR3	PCPR2	PCPR1	PCPR0
			R/W		R/W					
			0	0	0	0	0	0	0	0
			CTL Duty Discriminating Circuit Source Clock Selection 00 : TBC3 10 : TBC7 01 : TBC5 11 : TBC10		6-bit programmable clock divider control Divider setting 1/1 to 1/64 from CTLIN (from 30), CTLOUT (from CTL amp), CFGA (from CFG amp)					
CAPCR	Capture Control Register	FFBEH	CAP2T (CFG)	CAP1T (DFGPG)	CAPCL	VISFRS	VASFRS	TPRS0	CFGCL	CAFRS
			R	R	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			CAP2 Trigger Input Status 0 : No Trigger Input 1 : Trigger Input	CAP1 Trigger Input Status 0 : No Trigger Input 1 : Trigger Input	CAP1/CAP2 Status Clear 0 : – 1 : Clear	VISS Detection flag 0 : – 1 : Clear	VASS Detection flag 0 : – 1 : Clear	TPG0 FIFO Address 0 : – 1 : Clear	CFG flag Clear 0 : – 1 : Clear	CAP0 FIFO Counter / Status 0 : – 1 : Clear

6.2.11 Head Amp / Color Rotary Control Circuit

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
HACR	Head Amp Control Register	F794H	CRMOD R/W 0 CR/HA Outpit (P22/P23) COMPIN Input (P43) 0 : Disable 1 : Enable	"0" R/W 0 Always write "0"	VTPE34 R/W 0 VTP3 (P22) /VTP4 (P23) Trigger Edge Selection 0 : ↑ 1 : ↓	DFFPO1 R/W 0 TPG03 Input Polarity Switch 0 : Positive 1 : Negative	DFFPO0 R/W 0	COMPS R/W 0 COMPIN (P43) Input 0 : Disable 1 : Enable	CRPO R/W 0 CR Output Polarity Switch 0 : Positive 1 : Negative	HAPO R/W 0 HA Output Polarity Switch 0 : Positive 1 : Negative
P4MR	P4 Port Mode Register	F785H	$\overline{\text{AFFMIX}}$ R/W 0 AFF Signal (TPG01) Mix Control 0 : ON 1 : OFF	SCLK1E R/W 0 SCLK1 Output (P57) 0 : Disable 1 : Enable	RXD1E R/W 0 RXD1 Input (P45) 0 : Disable 1 : Enable	SWPE R/W 0 VASWP Output 0 : Disable 1 : Enable	BLKE R/W 0 BLK Output (P42) 0 : Disable 1 : Enable	TXD1E R/W 0 TXD1 Output (P42) 0 : Disable 1 : Enable	RGBE R/W 0 R/G/B Output 0 : Disable 1 : Enable	DOTXE R/W 0 Dot clock frequency (P40/P41) 0 : Disable 1 : Enable

6.2.12 Sync Signal Separator Circuit (CSYNC)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
CSYNCR	CSYNC Control Register	FFFDH	AVDPO R/W 0 VDIN Input Switch 0 : Positive 1 : Invert	AHDPO R/W 0 HDIN Input Switch 0 : Positive 1 : Invert	$\overline{\text{MDET1}}$ R 1 Mute Detection Flag 0 : Mute detection 1 : Normal	$\overline{\text{MDET0}}$ R 0 Mute Detection Flag 0 : Mute detection 1 : Normal	SYNCDET R 0 SYNC Signal Detection Flag 0 : Mute detection 1 : Normal	HSEN R/W 0 SYNC Control of H Pulse 0: Non-synchronize HP with Csync 1: Synchronize HP with Csync	MASK R/W 0 V.SYNC mask control 0 : – 1 : Release masking	
PWMCR	PWM Control Register	F793H		PWM01M R/W 0 PWM0/PWM1 Carrier Frequency 0 : 20.38 kHz 1 : 41.67 kHz	CFRTRGS R/W 0 CAPFR (P37) Trigger Edge Selection 0 : ↑ 1 : ↓	SYNCPO R/W 0 CSYNC Input Polarity Selection 0 : Positive 1 : Invert	PWMSEL R/W 0 PWM2/PWM3 (P74) Output Selection 0 : PWM2 1 : PWM3	PWMPO2 R/W 0 PWM2/PWM3 Output Polarity Selection 0 : Positive 1 : Invert	PWMPO1 R/W 0 PWM1 Output Polarity Selection 0 : Positive 1 : Invert	PWMPO0 R/W 0 PWM0 Output Polarity Selection 0 : Positive 1 : Invert

6.2.13 Psudo-Vsync Output Signal Circuit (PV / BLK)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
PVCR	PV Control Register	F799H	XOON R/W 0 XI/XO Oscillation or VDIN Input 0 : Disable 1 : Enable	N R/W 0 SC/SY Output (P46/P47) 0 : Disable 1 : Enable	"0" R/W 0 Always write "0"	$\overline{\text{BLKMIX}}$ R/W 0 With BLK Signal (from OSD) 0 : Mix 1 : Not mix	PHMIX R/W 0 With HP Signal (from CSYNC) 0 : Not mix 1 : Mix	PVSEL2 R/W 0 Select the output format PV Select the output format on 0 (H) to 7 (H)	PVSEL1 R/W 0	PVSEL0 R/W 0

6.2.14 On Screen Display Control (OSD)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
OSDCR	OSD Control Register	FFCEH	CMD1	CMD0	TCEN	DISPON	EXT/$\overline{INT}$	4/$\overline{3}$	50/$\overline{60}$	P/$\overline{N}$
			R/W		R/W	R/W	R/W	R/W		
			0	0	0	0	0	0	0	0
			Blinking mode is related with (ODSMR4) <MOD>.		Dot Clock (TC) Control 0 : Stop 1 : Enable	Display Output Enable 0 : Stop 1 : Enable	Display synchroniza-tion 0 : Interrnal mode 1 : External mode	Color Data Frequency Selection 0 : 3.58 MHz 1 : 4.43 MHz	Vertical Frequency Selection 0 : 60 Hz 1 : 50 Hz	PAL/NTSC 0 : NTSC 1 : PAL
OSDADR	Display RAM Address Setup Register	FFCFH	OSDA7	OSDA6	OSDA5	OSDA4	OSDA3	OSDA2	OSDA1	OSDA0
			R/W							
			0	0	0	0	0	0	0	0
			Address for Display RAM or OSD mode register (F0H to F7H)							
OSDDBR	Display RAM Data Buffer Register	FFD0H	OSDD7	OSDD6	OSDD5	OSDD4	OSDD3	OSDD2	OSDD1	OSDD0
			R/W							
			0	0	0	0	0	0	0	0
			Data buffer for Display RAM or OSD mode register (F0H to F7H)							
CHARD0 to CHARD239	Display RAM (character code register)	0000H to 00EFH	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
			W							
			*	*	*	*	*	*	*	*
			Character code (252 character code + 4 blank code)							
OSDMR0	OSD Mode Register 0	00F0H	POSV3	POSV2	POSV1	POSV0	POSH3	POSH2	POSH1	POSH0
			W				W			
			0	0	0	0	0	0	0	0
			Vertical start position Select 16 starting position (×4 – HD)				Horizontal start position Select 16 starting position (×4 – TC)			
OSDMR1	OSD Mode Register 1	00F1H	FSV1	FSV0	FSH1	FSH0	CSV1	CSV0	CSH1	CSH0
			W				W			
			0	0	0	0	0	0	0	0
			Character size of 1st line vertical size (×1, 2, 3, 4)		Character size of 1st line Horizonatal size (×1, 2, 3, 4)		Character size of 2nd to 10th line vertical size (×1, 2, 3, 4)		Character size of 2nd to 10th line Horizonatal size (×1, 2, 3, 4)	
OSDMR2	OSD Mode Register 2	00F2H	MSL3	MSL2	MSL1	MSL0	NSL3	NSL2	NSL1	NSL0
			W				W			
			0	0	0	0	0	0	0	0
			Mth Line				Nth Line			
OSDMR3	OSD Mode Register 3	00F3H	SPACE1	SPACE0	GLD1	GLD0	NLD1	NLD0	FLD1	FLD0
			W		W		W		W	
			0	0	0	0	0	0	0	0
			Line space 00 : 0HD 01 : 1HD 10 : 2HD 11 : 3HD		General flinking 0 : OFF 1 : ON	General back screen of character 0 : OFF 1 : ON	M to N line flinking 0 : OFF 1 : ON	M to N line back screen of character 0 : OFF 1 : ON	General flinking 0 : OFF 1 : ON	General back screen of character 0 : OFF 1 : ON

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
OSDMR4	OSD Mode Register 4	00F4H	CB/$\overline{CF}$	FCPH2	FDPH2	FEPH2	MOD	BLINK2	BLINK1	BLINK0
			W				W	W	W	
			0	0	0	0	0	0	0	0
			Color select by blinking code 0 : Character color 1 : Back screen color	PH2 of blank code FCH Coloring the characters (character background) depend on blank code FCH	PH2 of blank code FDH Coloring the characters (character background) depend on blank code FDH	PH2 of blank code FEH Coloring the characters (character background) depend on blank code FEH	Display character style Blinking mode is related with <CMD1, 0> bit in OSDCR register	Blinking time 0 : 2^5/fV [s] 1 : 2^6/fV [s]	Blinking duty 00 : Blinking OFF 01 : 1/4 duty 10 : 2/4 duty 11 : 3/4 duty	
OSDMR5	OSD Mode Register 5	00F5H	BGOFF	BGPH2	BGPH1	BGPH0	CBOFF	CBPH2	CBPH1	CBPH0
			W	W			W	W		
			0	0	0	0	0	0	0	0
			Color of back screen 0 : ON 1 : OFF	Coloring of back screen 8 colors at eact 45 deg. (0 to 7H)			Color of character background 0 : ON 1 : OFF	Coloring character backgound 8 colors at eact 45 deg. (0 to 7H)		
OSDMR6	OSD Mode Register 6	00F6H	"0"	YL2	YL1	YL0	CFOFF	CFPH2	CFPH1	CFPH0
			W	W			W	W		
			0	0	0	0	0	0	0	0
			Alway write "0"	Brightness level Selecting from 5 to 100 IRE			Coloring of character 0 : ON 1 : OFF	Character color 8 colors at each 45 deg. (0 to 7H)		
OSDMR7	OSD Mode Register 7	00F7H	SPON	SMOOTH	EQON	NONINT	RATIOHV	PVEN	AVDEN	AHDEN
			W	W	W	W		W	W	W
			0	0	0	0	0	0	0	0
			Character back screen between lines 0 : Disable 1 : Enable	Smoothing 0 : Disable 1 : Enable	Equivalent pulse in non-interlace 0 : ON 1 : OFF	Setting frquency ratio between VD and HD while full page mode The frequency ratio between HD and VD results from OSDCR <50 / 60>, <NOINT> and <RATIOHV>.		VD input switching 0 : VDIN or VSD from Csync 1 : TPG04	External VDIN Input 0 : Disable 1 : Enable	External HDIN Input 0 : Disable 1 : Enable
PVCR	PV Control Register	F799H	XOON	S/N	"0"	$\overline{BLKMIX}$	PHMIX	PVSEL2	PVSEL1	PVSEL0
			R/W	R/W	R/W	R/W	R/W	R/W		
			0	0	0	0	0	0	0	0
			XI/XO Oscillation or VDIN Input 0 : Disable 1 : Enable	SC/SY Output (P46/P47) 0 : Disable 1 : Enable	Always write "0"	With BLK Signal (from OSD) 0 : Mix 1 : Not mix	With HP Signal (from CSYNC) 0 : Not mix 1 : Mix	Select the output format PV Select the output format on 0 (H) to 7 (H)		
P4MR	P4 Port Mode Register	F785H	$\overline{AFFMIX}$	SCLK1E	RXD1E	SWPE	BLKE	TXD1E	RGBE	DOTXE
			R/W	R/W	R/W	R/W	R/W		R/W	
			0	0	0	0	0	0	0	0
			AFF signal mix control 0 : ON 1 : OFF	SCLK1 output 0 : Disable 1 : Enable	RXD1 input (P45) 0 : Disable 1 : Enable	VASWP output 0 : Disable 1 : Enable	BLK output (P42) 0 : Disable 1 : Enable	TXD1 output (P42) 0 : Disable 1 : Enable	R/G/B output R/W (P47/P46/P45) 0 : Disable 1 : Enable	Dot clock frequency 0 : Disable 1 : Enable
CSYNCR	CSYNC Control Register	FFFDH	AVDPO	AHDPO	$\overline{MDET1}$	$\overline{MDET0}$	SYNCDET	HSEN	MASK	
			R/W		R			R/W	R/W	
			0	0	1	0	0	0	0	
			VDIN Input Switch 0 : Positive 1 : Invert	HDIN Input Switch 0 : Positive 1 : Invert	Mute Detection Flag 0 : Mute detection 1 : Normal	Mute Detection Flag 0 : Mute detection 1 : Normal	SYNC Signal Detection Flag 0 : Mute detection 1 : Normal	SYNC Control of H Pulse 0: Non-synchronize HP with Csync 1: Synchronize HP with Csync	V.SYNC mask control 0 : – 1 : Release masking	

6.2.15 Serial Channel

(1) Serial channel 0 (SIO0)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
SC0CR	Serial Channel 0 Mode Register	FFDFH	FF0SI	S0RES	S0MD1	S0MD0	SIFT0	CLK0SI	SCK0S	SIO0E
			R	R/W	R/W		R/W	R/W	R/W	R/W
			1	0	0	0	0	0	0	0
			Serial transfer monitor flag 0 : In operation 1 : Stop	Serial transfer terminate 0 : – 1 : Terminate	Serial mode select 00 : Transmit mode 01 : Receive mode 10 : – 11 : Transmit/receive mode		Serial shift edge select 0 : Leading (Falling) edge 1 : Trailing (Rising) edge	Serial internal clock rate select 0 : TBC4 1 : TBC7	Serial clock select 0 : Internal clock 1 : External clock	Serial transfer enable / disable 0 : Disable 1 : Enable
SC0BR	Serial Channel 0 Buffer Register	FFDEH	TRB07	TRB06	TRB05	TRB04	TRB03	TRB02	TRB01	TRB00
			R/W							
			*	*	*	*	*	*	*	*

(2) Serial channel 1 (SIO1)

SYMBOL	NAME	Addr	7	6	5	4	3	2	1	0
SC1CR	Serial Channel 1 Mode Register	FFE1H	FF1SI	S1RES	S1MD1	S1MD0	SIFT1	CLK1SI	SCK1S	SIO1E
			R	R/W	R/W		R/W	R/W	R/W	R/W
			1	0	0	0	0	0	0	0
			Serial transfer monitor flag 0 : In operation 1 : Stop	Serial transfer terminate 0 : – 1 : Terminate	Serial mode select 00 : Transmit mode 01 : Receive mode 10 : – 11 : Transmit/receive mode		Serial shift edge select 0 : Leading (Falling) edge 1 : Trailing (Rising) edge	Serial internal clock rate select 0 : TBC4 1 : TBC7	Serial clock select 0 : Internal clock 1 : External clock	Serial transfer enable / disable 0 : Disable 1 : Enable
SC1BR	Serial Channel 1 Buffer Register	FFE0H	TRB17	TRB16	TRB15	TRB14	TRB13	TRB12	TRB11	TRB10
			R/W							
			*	*	*	*	*	*	*	*

6.2.16 Serial Bus Interface (SBI)

(1) I²C BUS Mode

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
SBICR1	Serial Bus Interface Control Register 1	FFE2H	"0"	"0"	"0"	ACK	CHS	SCK		
			W			R/W	R/W	W		
						0	0	0	0	0
			Always write "0"	Always write "0"	Always write "0"	Set of Acknowledge bit 0 : Output 1 to SDA 1 : Output 0 to SDA	I/O channel selection 0 : Channel 0 (SCL0 / SDA0) 1 : Channel 1 (SCL1 / SDA1)	Frequency (f_{SCL}) of Serial Clock Selection 000 : fc/2^6 (250 kHz) 100 : fc/2^{10} (15.6 kHz) 001 : fc/2^7 (125 kHz) 101 : fc/2^{11} (7.8 kHz) 010 : fc/2^8 (62.5 kHz) 110 : fc/2^{12} (3.9 kHz) 011 : fc/2^9 (31.2 kHz) 111 : –		
SBIDBR	Serial Bus interface Data Buffer Register	FFE3H	DBRD7	DBRD6	DBRD5	DBRD4	DBRD3	DBRD2	DBRD1	DBRD0
			R/W							
			0	0	0	0	0	0	0	0
			Data Buffer							
I2CAR	I²C BUS Address Register	FFE4H	SA6	SA5	SA4	SA3	SA2	SA1	SA0	ALS
			W							
			0	0	0	0	0	0	0	0
			Slave Address							Address recognition mode specification 0 : Recognized 1 : Not recognized
SBICR2	Serial Bus Interface Control Register 2	FFE5H	MST	TRK	BB	PIN	SBIM		"0"	"0"
			R/W	R/W	R/W	R/W	W		W	
			0	0	0	1	0	0	*	*
			(W) Master / slave selection, (R) Status monitor 0 : Slave 1 : Master	(W) Transmit / receive selection, (R) Status monitor 0 : Receiver 1 : Transmitter	(W) Start / stop generation, (R) I²C bus status monitor 0 : (W) Stop condition, (R) Bus free 1 : (W) Start condition, (R) Bus busy	(W) Clear interrupt service request (R) Monitor interrupt service request state 0 : (W) – (R) Interrupt service being request 1 : (W) Interrupt service request cleared (R) Cleared state	Serial bus interface operating mode selection 00 : Port mode (serial bus interface output disable) 01 : SIO mode 10 : I²C bus mode 11 : Don't use		Always write "0"	Always write "0"

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
								AAS	AD0	LRB
								R	R	R
			*	*	*	*	*	*	*	*
SBISR	Serial Bus Interface Status Register	FFE5H						Slave address match detection monitor 0 : – 1 : Slave address match or "GENERAL CALL" detected	"GENERAL CALL" detection monitor 0 : – 1 : "GENERAL CALL" detected	Last received bit monitor 0 : Last received bit "0" 1 : Last received bit "1"

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
I2CFCR1	I²C BUS FIFO Control Register 1	FFE6H	T/$\overline{R}$	FSCK			CONT	BYTE		
			W	W			W	W		
			0	0	0	0	0	0	0	0
			FIFO transfer mode selection 0 : Receive mode 1 : Transmit mode	Serial clock frequency (fSCL) selection 000 : fc/2^6 (250 kHz) 100 : fc/2^{10} (15.6 kHz) 001 : fc/2^7 (125 kHz) 101 : fc/2^{11} (7.8 kHz) 010 : fc/2^8 (62.5 kHz) 110 : fc/2^{12} (3.9 kHz) 011 : fc/2^9 (31.2 kHz) 111 : –			Data transfer mode 0 : 8-byte data transfer mode 1 : Continue transfer	Number of transfer words 000 : 1 Byte 100 : 5 Byte 001 : 2 Byte 101 : 6 Byte 010 : 3 Byte 110 : 7 Byte 011 : 4 Byte 111 : 8 Byte		
I2CFCR2	I²C BUS FIFO Control Register 2	FFE7H	$\overline{START}$	$\overline{STOP}$	CHS	$\overline{INT}$			$\overline{RST}$	
			W	W	W	W			W	
			1	1	0	1	*	*	1	*
			FIFO Buffer Transfer Start 0 : Start or Restart 1 : –	FIFO buffer Stop 0 : Stop 1 : –	I/O channel selection 0 : Channel 0 (SCL0, SDA0) 1 : Channel 1 (SCL1, SDA1)	Next transfer start of continue data trans mode 0 : Next transfer start 1 : –			I²C BUS or FIFO ctonrol circuit system reset 0 : Reset 1 : –	
I2CFSR1	I²C BUS FIFO Status Register 1	FFE7H	SDA	END	CHS	BUSY	FULL	EMPTY	ERROR	AKERR
			R							
			*	0	0	0	0	0	0	0
			SDA bus monitor 0 : SDA line is low level 1 : SDA line is high level	FIFO buffer status flag 0 : – 1 : Transfer	I/O channel monitor 0 : Channel 0 1 : Channel 1	FIFO buffer transfer status monitor 0 : – 1 : Transfer	FIFO buffer full / receive end monitor 0 : – 1 : FIFO buffer-full / receive end	FIFO buffer empty / transfer-end monitor 0 : – 1 : FIFO buffer empty / transfer-end	Detect of start condition error 0 : – 1 : Error	Detect Acknowledge error 0 : – 1 : Error
I2CFDBR	I²C BUS FIFO Data Buffer Register	FFE8H	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
			R/W							
			*	*	*	*	*	*	*	*
			FIFO Buffer Register							
I2CFSR2	I²C BUS FIFO Status Register 2	FFE9H	NOMAT	LRBM						
			R							
			0	1						
			SCL pin output and SCL line match monitor 0 : – 1 : SCL line is "L" level by slave device	Last received bit monitor 0 : Last received bit "0" 1 : Last received bit "1"						

(2) SIO mode

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
SBICR1	Serial Bus Interface Control Register 1	FFE2H	SIOS	SIOINH	SIOM		CHS	SCK		
			W	W	W		R/W	W		
			0	0	0	0	0	0	0	0
			Transfer start / stop 0 : Stop 1 : Start	Transfer forced stop 0 : – 1 : Forced stop	Transfer mode selection 00 : Transmit mode 01 : Don't use 10 : Transmit / receive mode 11 : receive mode		I/O channel selection 0 : Channel 0 (SCLK2, TXD2, RXD2) 1 : –	Serial clock frequency selection 000 : $fc/2^6$ (250 kHz) 100 : $fc/2^{10}$ (15.6 kHz) 001 : $fc/2^7$ (125 kHz) 101 : $fc/2^{11}$ (7.8 kHz) 010 : $fc/2^8$ (62.5 kHz) 110 : $fc/2^{12}$ (3.9 kHz) 011 : $fc/2^9$ (31.2 kHz) 111 : External clock		
SBIDBR	Serial Bus Interface Data Buffer Register	FFE3H	DBRD7	DBRD6	DBRD5	DBRD4	D8RD3	DBRD2	DBRD1	DBRD0
			R/W							
			*	*	*	*	*	*	*	*
			Data Buffer							
SBICR2	Serial Bus Interface Control Register 2	FFE5H	"0"	"0"	"0"	"1"	SBM		"0"	"0"
			W							
			*	*	*	*	0	0	*	*
			Always write "0"			Always write "1"	Serial bus interface operation mode selection 00 : Port mode 01 : SIO mode 10 : I²C bus mode 11 : Don't use		Always write "0"	
SBISR	Serial bus Interface Status Register	FFE5H					SIOF	SEF		
							R			
			*	*	*	*	0	0	*	*
							Serial transfer operating status monitor 0 : Transfer terminated 1 : Transfer in process	Shift operating status monitor 0 : Shift operation terminated 1 : Shift operation in process		

6.2.17 8-bit A/D Converter Circuit (A/D)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
ADMOD	A/D Converter Control Register	FFDCH	"1"	EOCF	ADBF	ADS	ADCH3	ADCH2	ADCH1	ADCH0
			R/W	R		R/W	R/W			
			1	0	0	0	0	0	0	0
			Always write "1"	A/D conversion flag 0 : A/D conversion in process 1 : A/D conversion terminat-ed	A/D conversion busy flag 0 : A/D conversion non-busy (stop) 1 : A/D conversion busy	A/D conversion start 0 : – 1 : A/D conversion start	Analog channel selection 0000 : AIN0 0011 : AIN3 0110 : AIN6 1001 : AIN9 0001 : AIN1 0100 : AIN4 0111 : AIN7 1010 : PDP 0010 : AIN2 0101 : AIN5 1000 : AIN8 1011 : PDM (11** : reserved)			
ADREG	A/D Comparato r Register	FFDDH	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
			R							
			*	*	*	*	*	*	*	*

6.2.18 Servo Control Amplifier

(1) CTL Amplifier

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
SACR1	Servo Amp Control Register 1	FFF1H	DIRE	DIRFLG	CTLPO	CTRGE	PDMON	PDPON	INDEX	REC
			R/W	R	R/W	R/W	R/W	R/W	R/W	
			0	0	0	0	0	0	0	
			INTDIR interrupt request 0 : Disable 1 : Enable	DIR detection flag 0 : CFGB ahead of CFGA 1 : CFGA ahead of CFGB	Polarity switch of CTL 0 : Positive (forward) 1 : Invert (reverse)	CTLOUT auto-reset function 0 : OFF 1 : ON	CTL (−) shumit selection 0 : Manual 1 : Peak hold	CTL (+) shumit selection 0 : Manual 1 : Peak hold	Record mode 00 : Reproducing mode *1 : Recording mode 10 : Index mode	
SACR2	Servo Amp Control Register 2	FFF2H	PHSPUP	CAMP2	CAMP1	CAMP0	SMTM1	SMTM0	SMTP1	SMTP0
			R/W	R/W	R/W	R/W	R/W		R/W	
			0	0	0	0	0	0	0	0
			Peak-hold mode select 0 : Normal recovery 1 : High speed recovery	CTL Amp 2 switch 0 : OFF 1 : ON	CTL Amp 1 switch 0 : OFF 1 : ON	CTL Amp 0 switch 0 : OFF 1 : ON	CTL Schmitt plus level manual select 00 : − 100 mV 10 : − 300 mV 01 : − 200 mV 11 : − 500 mV		CTL Schmitt plus level manual select 00 : + 100 mV 10 : + 300 mV 01 : + 200 mV 11 : + 500 mV	
SACR3	Servo Amp Control Register 3	FFF3H	IDIRS	SWPTB	SWPTA	AOUTS1	AOUTS0	CFGBS	CFGAS	SWSHT
			R/W	R/W		R/W		R/W		R/W
			0	0	0	0	0	0	0	0
			INTDIR input select 0 : DIRFLG 1 : CFGB	SWPB timing selection in index mode 00 : 1.5 ms 10 : 2.5 ms 01 : 2.0 ms 11 : 3.0 ms		AMPOUT (P30) output source select 00 : CTLOUT 10 : CFGB 01 : CFGA 11 : Don't use		CFGB amp shumit level 0 : ± 80 mv 1 : ± 120 mV	CFGA amp shumit level 0 : ± 80 mV 1 : ± 120 mV	SWBS select 0 : Automatic control 1 : Always "ON"
SACR4	Servo Amp Control Register 4	F796H	"0"	"0"	"0"	"0"	CFGBZ	CFGAZ	CFGPO	CTLOUT
			R/W				R/W	R/W	R/W	R
			0	0	0	0	0	0	0	*
			Always write "0"				FGB Schmit select 0 : Zero cross Schmit 1 : Manual Schmit	FGA Schmit select 0 : Zero cross Schmit 1 : Manual Schmit	Zero cross polarity select 0 : Positive 1 : Negative	CTL amp output status 0 : CTLOUT = "0" 1 : CTLOUT = "1"

(2) CFG Amplifier

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
SACR1	Servo Amp Control Register 1	FFF1H	DIRE	DIRFLG	CTLPO	CTRGE	PDMON	PDPON	INDEX	REC
			R/W	R	R/W	R/W	R/W	R/W	R/W	
			0	0	0	0	0	0	0	
			INTDIR interrupt request 0 : Disable 1 : Enable	DIR detection flag 0 : CFGB ahead of CFGA 1 : CFGA ahead of CFGB	Polarity switch of CTL 0 : Positive (forward) 1 : Invert (reverse)	CTLOUT auto-reset function 0 : OFF 1 : ON	CTL (−) shumit selection 0 : Manual 1 : Peak hold	CTL (+) shumit selection 0 : Manual 1 : Peak hold	Record mode 00 : Reproducing mode *1 : Recording mode 10 : Index mode	
SACR3	Servo Amp Control Register 3	FFF3H	IDIRS	SWPTB	SWPTA	AOUTS1	AOUTS0	CFGBS	CFGAS	SWSHT
			R/W	R/W		R/W		R/W		R/W
			0	0	0	0	0	0	0	0
			INTDIR input select 0 : DIRFLG 1 : CFGB	SWPB timing selection in index mode 00 : 1.5 ms 10 : 2.5 ms 01 : 2.0 ms 11 : 3.0 ms		AMPOUT (P30) output source select 00 : CTLOUT 10 : CFGB 01 : CFGA 11 : Don't use		CFGB amp shumit level 0 : ±80 mv 1 : ±120 mV	CFGA amp shumit level 0 : ±80 mV 1 : ±120 mV	SWBS select 0 : Automatic control 1 : Always "ON"
SACR4	Servo Amp Control Register 4	F796H	"0"	"0"	"0"	"0"	CFGBZ	CFGAZ	CFGPO	CTLOUT
			R/W				R/W	R/W	R/W	R
			0	0	0	0	0	0	0	*
			Always write "0"				FGB Schmit select 0 : Zero cross Schmit 1 : Manual Schmit	FGA Schmit select 0 : Zero cross Schmit 1 : Manual Schmit	Zero cross polarity select 0 : Positive 1 : Negative	CTL amp output status 0 : CTLOUT = "0" 1 : CTLOUT = "1"

6.2.19 Port

(1) P0 port

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P0	P0 port Data Register	FFC0H	P07	P06	P05	P04	P03	P02	P01	P00
			R/W							
			0	0	0	0	0	0	0	0
P0CR	P0 port Control Register	FFC1H	P07C	P06C	P05C	P04C	P03C	P02C	P01C	P00C
			W							
			0	0	0	0	0	0	0	0
			P1 port I/O Control 0 : Input mode 1 : Output mode							

(2) P1 port

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P1	P1 port Data Register	FFC2H	P17	P16	P15	P14	P13	P12	P11	P10
			R/W							
			0	0	0	0	0	0	0	0
P1CR	P1 port Control Register	FFC3H	P17C	P16C	P15C	P14C	P13C	P12C	P11C	P10C
			W							
			0	0	0	0	0	0	0	0
			P1 port I/O Control 0 : Input mode 1 : Output mode							

(3) P2 port (1/2)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P2	P2 port Data Register	FFC4H	P27	P26	P25	P24	P23	P22	P21	P20
			R/W							
			0	0	0	0	0	0	0	0
P2CR	P2 port Control Register	F7B0H	P27C	P26C	P25C	P24C	P23C	P22C	P21C	P20C
			R/W							
			0	0	0	0	0	0	0	0
			P2 port I/O Control 0 : Input mode 1 : Output mode							
P2MR	P2 port Mode Register	F781H	RXD0E	TXD0E	SCLK0E	TP2E	TP1E	TP0E	TPG01E	TPG00E
			R/W							
			0	0	0	0	0	0	0	0
			RXD0 Input (P27) 0 : Disable 1 : Enable	TXD0 Output (P26) 0 : Disable 1 : Enable	SCLK0 I/O (P25) 0 : Disable 1 : Enable	TP2 Output (P24) 0 : Disable 1 : Enable	TP1 Output (P21) 0 : Disable 1 : Enable	TP0 Output (P20) 0 : Disable 1 : Enable	TPG01 Output (P21) 0 : Disable 1 : Enable	TPG00 Output (P20) 0 : Disable 1 : Enable
P3MR	P3 port Mode Register	F783H	VTP4E	VTP3E	CAPFRD	CAPFRD	TPG12E	TP3E	TO3E	CTLCFGE
			R/W		R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			VTP4 Output (P23) 0 : Disable 1 : Enable	VTP3 Output (P22) 0 : Disable 1 : Enable	CAPFR (P37) Data Register	CAPER Output (P37) 0 : Disable 1 : Enable	TPG12 Output (P36) 0 : Disable 1 : Enable	TP3 Output (P36) 0 : Disable 1 : Enable	TO3 Output (P35) 0 : Disable 1 : Enable	AMP Output (P30) 0 : Disable 1 : Enable

(3) P2 port (2/2)

SYMBOLP	NAMEP	Addr.	7	6	5	4	3	2	1	0
TPCR	TP Control Register	FFDAH	TPE3	VASEL3	TPE2	VASEL2	TPE1	VASEL1	TPE0	VASEL0
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			TP3 (P36) Trigger Edge Selection 0 : ↑ 1 : ↓	TP3 (P36) Trigger Selection 0 : TPG03 1 : TPG01	TP2 (P24) Trigger Edge Selection 0 : ↑ 1 : ↓	TP2 (P24) Trigger Selection 0 : TPG03 1 : TPG01	TP1 (P21) Trigger Edge Selection 0 : ↑ 1 : ↓	TP1 (P21) Trigger Selection 0 : TPG03 1 : TPG01	TP0 (P20) Trigger Edge Selection 0 : ↑ 1 : ↓	TP0 (P20) Trigger Selection 0 : TPG03 1 : TPG01
TPDR	TP Data Register	FFDBH	VTP3D	VTP2D	VTP1D	VTP0D	TP3D	TP2D	TP1D	TP0D
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			VTP3 (P22) Data Register	VTP2 (P54) Data Register	VTP1 (P53) Data Register	VTP0 (P52) Data Register	TP3 (P36) Data Register	TP2 (P24) Data Register	TP1 (P21) Data Register	TP0 (P20) Data Register
P7	P7 Port Data Register	FFC9H			VTP4D	P74	P73	P72	P71	P70
					R/W	R/W	R/W	R/W	R	R
					0	0	0	0	*	*
					VTP4 (P23) Data Register	P74 Data Register	P73 Data Register	P72 Data Register	P71 Data Register	P70 Data Register
HACR	Head Amp Control Register	F794H	CRMOD	"0"	VTPE34	DFFP01	DFFP01	COMPS	CRPO	HAPO
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			CR / HA Output (P21 / P23) COMPIN input (P43) 0 : Disable 1 : Enable	Always write "0"	VTP3 (P22) /VTP4 (P23) Trigger Edge Selection 0 : ↑ 1 : ↓	TPG03 Input Polarity Switch 0 : Positive 1 : Negative		COMPIN (P43) Input 0 : Disable 1 : Enable	CR Output Polarity Switch 0 : Positive 1 : Negative	HA Output Polarity Switch 0 : Positive 1 : Negative
ODMCR1	Open-drain Control Register	F789H	PWM1OC	PWM0OC	P37OC	P24OC	P23OC	P22OC	P21OC	P20OC
			R/W		R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			PWM1 Output Control 0 : Puch-Pull 1 : Open-drain	PWM0 Output Control 0 : Puch-Pull 1 : Open-drain	P37 Output 0 : Puch-Pull 1 : Open-drain	P24 Output 0 : Puch-Pull 1 : Open-drain	P23 Output 0 : Puch-Pull 1 : Open-drain	P22 Output 0 : Puch-Pull 1 : Open-drain	P21 Output 0 : Puch-Pull 1 : Open-drain	P20 Output 0 : Puch-Pull 1 : Open-drain

(4) P3 port (1/2)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P3	P3 port Data Register	FFC5H	P37	P36	P35	P34	P33	P32	P31	P30
			R/W							
			0	0	0	0	0	0	0	0
P3CR	P3 port Control Register	F782H	P37C	P36C	P35C	P34C	P33C	P32C	P31C	P30C
			R/W							
			0	0	0	0	0	0	0	0
			P3 port I/O Control 0 : Input mode 1 : Output mode							

(4) P3 port (2/2)

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P3MR	P3 port Mode Register	F783H	VTP4E	VTP3E	CAPFRD	CAPFR	TPG12E	TP3E	TO3E	CTLCFGE
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			VTP4 Output (P23) 0 : Disable 1 : Enable	VTP3 Output (P22) 0 : Disable 1 : Enable	CAPFR (P37) Data Register	CAPER Output (P37) 0 : Disable 1 : Enable	TPG12 Output (P36) 0 : Disable 1 : Enable	TP3 Output (P36) 0 : Disable 1 : Enable	TO3 Output (P35) 0 : Disable 1 : Enable	AMPOUT (P30) 0 : Disable 1 : Enable
PWMCR	PWM Control Register	F793H		PWM01M	CFRTRGS	SYNCPO	WPMSEL	PWMPO2	PWMPO1	PWMPO0
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
				0	0	0	0	0	0	0
				PWM0/PWM1 Carrier Frequency Selection 0 : 20.83 kHz 1 : 41.67 kHz	CAPFR (P37) Trigger Edge Selection 0 : ↑ 1 : ↓	CSYNC Input Polarity Selection 0 : Positive 1 : Invert	PWM2/PWM3 Output (P74) Selection 0 : PWM2 1 : PWM3	PWM2/PWM3 Output Polarity Selection 0 : Positive 1 : Invert	PWM1 Output Polarity Selection 0 : Positive 1 : Invert	PWM0 Output Polarity Selection 0 : Positive 1 : Invert
TPCR	TP Control Register	FFDAH	TPE3	VASEL3	TPE2	VASEL2	TPE1	VASEL1	TPE0	VASEL0
			R/W		R/W					
			0	0	0	0	0	0	0	0
			TP3 (P36) Trigger Edge Selection 0 : ↑ 1 : ↓	TP3 (P36) Trigger Selection 0 : TPG03 1 : TPG01	TP2 (P24) Trigger Edge Selection 0 : ↑ 1 : ↓	TP2 (P24) Trigger Selection 0 : TPG03 1 : TPG01	TP1 (P21) Trigger Edge Selection 0 : ↑ 1 : ↓	TP1 (P21) Trigger Selection 0 : TPG03 1 : TPG01	TP0 (P20) Trigger Edge Selection 0 : ↑ 1 : ↓	TP0 (P20) Trigger Selection 0 : TPG03 1 : TPG01
TPDR	TP Data Register	FFDBH	VTP3D	VTP2D	VTP1D	VTP0D	TP3D	TP2D	TP1D	TP0D
			R/W	R/W			R/W	R/W		
			0	0	0	0	0	0	0	0
			VTP3 (P22) Data Register	VTP2 (P54) Data Register	VTP1 (P53) Data Register	VTP0 (P52) Data Register	TP3 (P36) Data Register	TP2 (P24) Data Register	TP1 (P21) Data Register	TP0 (P20) Data Register
HACR	Head Amp Control Register	F794H	CRMOD	"0"	VTPE34	DFFP01	DFFP01	COMPS	CRPO	HAPO
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			CR / HA Output (P22/P23) COMPIN Input (P43) 0 : Disable 1 : Enable	Always write "0"	VTP3 (P22) /VTP4 (P23) Trigger Edge Selection 0 : ↑ 1 : ↓	TPG03 Input Polarity Switch 0 : Positive 1 : Negative		COMPIN (P43) Input 0 : Disable 1 : Enable	CR Output Polarity Switch 0 : Positive 1 : Negative	HA Output Polarity Switch 0 : Positive 1 : Negative
ODMCR1	Open-drain Control Register	F789H	PWM1OC	PWM0OC	P37OC	P24OC	P23OC	P22OC	P21OC	P20OC
			R/W		R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			PWM1 Output Control 0 : Puch-Pull 1 : Open-drain	PWM0 Output Control 0 : Puch-Pull 1 : Open-drain	P37 Output 0 : Puch-Pull 1 : Open-drain	P24 Output 0 : Puch-Pull 1 : Open-drain	P23 Output 0 : Puch-Pull 1 : Open-drain	P22 Output 0 : Puch-Pull 1 : Open-drain	P21 Output 0 : Puch-Pull 1 : Open-drain	P20 Output 0 : Puch-Pull 1 : Open-drain

(5) P4 port

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P4	P4 Port Data Register	FFC6H	P47	P46	P45	P44	P43	P42	P41	P40
			R/W							
			0	0	0	0	0	0	0	0
P4CR	P4 Port Control Register	F784H	P47C	P46C	P45C	P44C	P43C	P42C	P41C	P40C
			R/W							
			0	0	0	0	0	0	0	0
			P4 Port Input / Output Control 0 : Input mode 1 : Output mode							
P4MR	P4 Port Mode Register	F785H	$\overline{\text{AFFMIX}}$	SCLK1E	RXD1E	SWPE	BLKE	TXD1E	RGBE	DOTXE
			R/W	R/W	R/W	R/W	R/W			
			0	0	0	0	0	0	0	0
			AFF signal mix control 0 : ON 1 : OFF	SCLK1 output 0 : Disable 1 : Enable	RXD1 input (P45) 0 : Disable 1 : Enable	VASWP output 0 : Disable 1 : Enable	BLK output (P42) 0 : Disable 1 : Enable	TXD1 output (P42) 0 : Disable 1 : Enable	R/G/B output (P47/P46/P45) 0 : Disable 1 : Enable	Dot clock frequency (P40/P41) 0 : Disable 1 : Enable
HACR	Head-amp Control Register	F794H	CRMOD	"0"	VTPE34	DFFPO1	DFFPO0	COMPSEL	CRPO	HAPO
			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			CA/HA output (P22/P23) COMPIN input (P43) 0 : Disable 1 : Enable	Always write "0"	VTP3 (P22) /VTP4 (P23) Trigger edge selection 0 : ↑ 1 : ↓	TPG03 input polarity switch 0 : Positive 1 : Negative	TPG03 input polarity switch 0 : Positive 1 : Negative	COMPIM (P43) input 0 : Disable 1 : Enable	CR output polarity switch 0 : Positive 1 : Negative	HA output polarity switch 0 : Positive 1 : Negative
PVCR	PV Control Register	F799H	XOON	S/N	"0"	$\overline{\text{BLKMIX}}$	PHMIX	PVSEL2	PVSEL1	PVSEL0
			R/W	R/W	R/W	R/W	R/W	R/W		
			0	0	0	0	0	0	0	0
			XI/XO oscillation or VDIN input 0 : Disable 1 : Enable	SC/SY output (P46/P47) 0 : Disable 1 : Enable	Always write "0"	With BLK signal (from OSD) 0 : Mix 1 : Not mix	With HP signal (from CSYNC) 0 : Not mix 1 : Mix	Select the output format PV/BLK. Select the output format on 0 (H) to 7 (H).		

(6) P5 port

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P5	P5 port Data Register	FFC7H	P57	P56	P55	P54	P53	P52	P51	P50
			R/W							
			0	0	0	0	0	0	0	0
P5CR	P5 port Control Register	F786H	P57C	P56C	P55C	P54C	P53C	P52C	P51C	P50C
			R/W							
			0	0	0	0	0	0	0	0
			P5 port I/O Control 0 : Input mode 1 : Output mode							
P5MR	P5 port Mode Register	F787H	VTPE2	VTPE1	VTPE0	VTPS2	VTPS1	VTPS0	INT1E	INT0E
			R/W							
			0	0	0	0	0	0	0	0
			VTP2 (P54) Trigger Edge Selection 0 : ↑ 1 : ↓	VTP1 (P53) Trigger Edge Selection 0 : ↑ 1 : ↓	VTP0 (P52) Trigger Edge Selection 0 : ↑ 1 : ↓	VTP2 Output (P54) 0 : Disable 1 : Enable	VTP1 Output (P53) 0 : Disable 1 : Enable	VTP0 Output (P52) 0 : Disable 1 : Enable	INT1 (P51) Intterrupt Edge Detect 0 : ↑ 1 : ↓	INT0 (P50) Intterrupt Edge Detect 0 : ↑ 1 : ↓
P4MR	P4 port Mode Register	F785H	$\overline{\text{AFFMIX}}$	SCLK1E	RXD1E	SWPE	BLKE	TXD1E	RGBE	DOTXE
			R/W	R/W	R/W	R/W	R/W			
			0	0	0	0	0	0	0	0
			AFF Signal Mix Control 0 : ON 1 : OFF	SCLK1 Output (P57) 0 : Disable 1 : Enable	RXD1 Input (P45) 0 : Disable 1 : Enable	VASWP Output 0 : Disable 1 : Enable	BLK Output (P42) 0 : Disable 1 : Enable	TXD1 Output (P42) 0 : Disable 1 : Enable	R/G/B Output (P47/P46/P45) 0 : Disable 1 : Enable	Dot clock frequency (P41/P40) 0 : Disable 1 : Enable
TPDR	TP Data Register	FFDBH	VTP3D	VTP2D	VTP1D	VTP0D	TP3D	TP2D	TP1D	TP0D
			R/W	R/W			R/W	R/W		
			0	0	0	0	0	0	0	0
			VTP3 (P22) Data Register	VTP2 (P54) Data Register	VTP1 (P53) Data Register	VTP0 (P52) Data Register	TP3 (P36) Data Register	TP2 (P24) Data Register	TP1 (P21) Data Register	TP0 (P20) Data Register
ODMCR2	Open-drain Control Register	F78AH				P74OC	P56OC	P55OC	P53OC	P52OC
						R/W	R/W	R/W	R/W	R/W
						0	0	0	0	0
						P74 Output 0 : Push-Pull 1 : Open-drain	P56 Output 0 : Push-Pull 1 : Open-drain	P55 Output 0 : Push-Pull 1 : Open-drain	P53 Output 0 : Push-Pull 1 : Open-drain	P52 Output 0 : Push-Pull 1 : Open-drain

(7) P6 port

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P6	P6 port Data Register	FFC8H	P67	P66	P65	P64	P63	P62	P61	P60
			R							
			-	-	-	-	-	-	-	-

(8) P7 port

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P7	P7 port Data Register	FFC9H			VTP4D	P74	P73	P72	P71	P70
					R/W	R/W			R/W	
					0	0	0	0	*	*
					VTP4 (P23) Data register	P74 Data register	P73 Data register	P72 Data register	P71Data register	P70Data register
P7CR	P7 port Control Register	F788H			P74M	P74C	P73C	P72C		
					R/W					
					0	0	0	0		
					PWM2/PWM3 Output (P74) 0 : Disable 1 : Enable	P74 Output Control 0 : Disable 1 : Enable	P73 I/O Control 0 : Input mode 1 : Output mode	P72 I/O Control 0 : Input mode 1 : Output mode		
PWMCR	PWM Control Register	F793H		PWM01M	CFRTRGS	SYNCPO	PWMSEL	PWMPO2	PWMPO1	PWMPO0
				R/W	R/W	R/W	R/W	R/W	R/W	R/W
				0	0	0	0	0	0	0
				PWM0/PWM1 Carrier Frequency Selection 0 : 20.83 kHz 1 : 41.67 kHz	CAPFR (P37) Trigger Edge Selection 0 : ↑ 1 : ↓	CSYNC INPUT Polarity Selection 0 : Positive 1 : Invert	PWM2/PWM3 (P74) Output Selection 0 : PWM2 1 : PWM3	PWM2/PWM3 Output Polarity Selection 0 : Positive 1 : Invert	PWM1 Output Polarity Selection 0 : Positive 1 : Invert	PWM0 Output Polarity Selection 0 : Positive 1 : Invert
TRUN	Timer Start Control Register	FFD4H	PWM3RUN	T3RUN	PWM1RUN	PWM0RUN	PWM2RUN	T2RUN	T1RUN	T0RUN
			R/W	R/W	R/W		R/W	R/W	R/W	R/W
			0	0	0	0	0	0	0	0
			PWM3 0 : Stop 1 : Start	TC3 0 : Stop 1 : Start	PWM1 Output Control 0 : Stop 1 : Start	PWM0 Output Control 0 : Stop 1 : Start	PWM2 0 : Stop 1 : Start	TC2 Output Control 0 : Stop 1 : Start	TC1 Output Control 0 : Stop 1 : Start	TC0 Output Control 0 : Stop 1 : Start
ODMCR2	Open-drain Control Register	F78AH				P74OC	P56OC	P55OC	P53OC	P52OC
						R/W	R/W	R/W		
						0	0	0	0	0
						P74 Output 0 : Puch-Pull 1 : Open-drain	P56 Output 0 : Puch-Pull 1 : Open-drain	P55 Output 0 : Puch-Pull 1 : Open-drain	P53 Output 0 : Puch-Pull 1 : Open-drain	P52 Output 0 : Puch-Pull 1 : Open-drain

(9) P8 port

SYMBOL	NAME	Addr.	7	6	5	4	3	2	1	0
P8	P8 port Data Register	FFB4H							P81	P80
									R/W	
									0	0